United States District Court,
N.D. California, San Jose Division.

RAMBUS INC,
Plaintiff.
v.
HYNIX SEMICONDUCTOR INC., Hynix Semiconductor America Inc., Hynix Semiconductor Manufacturing America Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P., Nanya Technology Corporation, Nanya Technology Corporation U.S.A,
Defendants.
Rambus Inc,
Plaintiff.
v.
Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P,
Defendants.
Rambus Inc,
Plaintiff.
v.
Micron Technology, Inc., and Micron Semiconductor Products, Inc,
Defendants.

Nos. C-05-00334 RMW, C-05-02298 RMW, C-06-00244 RMW

July 25, 2008.

CLAIM CONSTRUCTION ORDER FOR THE WARE PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTION FOR SUMMARY JUDGMENT

RONALD M. WHYTE**, District Judge.**

Rambus has accused the Manufacturers of infringing various patents. This order addresses two of the patents, U.S. Patent No. 6,496,897 and 6,493,789, which the parties refer to as the "Ware patents." FN1 In accord with the local rules, the parties have submitted their joint claim construction statement. Rambus has filed its opening and responding Markman FN2 briefs, motions for summary judgment of infringement, and oppositions to the Manufacturers' motions for summary judgment. The Manufacturers have filed their responsive *Markman* brief, oppositions to Rambus's summary judgment motions, and their own motions for summary judgment of non-infringement and invalidity. The court has reviewed the papers and considered the arguments of counsel and now sets forth its claim construction and rulings on the summary judgment motions dealing with the Ware patents.

FN1. The court previously construed the claims of the other fifteen patents-in-suit in a separate order. *See*

Rambus Inc. v. Hynix Semiconductor Inc., 2008 WL 2754805 (N.D.Cal.2008). That order contains additional background on DRAM technology and the present dispute between Rambus and the Manufacturers.

FN2. Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996).

I. BACKGROUND OF THE INVENTION

The two patents addressed by this order descend from application no. 08/545294, filed by Fred Ware, Craig Hampel, Donald Stark, and Matthew Griffin. Unlike the other patents-in-suit, the Ware patents have not been previously construed. Because the Ware patents share the same specification, the court refers to the specification of the '789 patent.

A. Technology Background-Write Masking

1. The Role of WE Signals in the DRAM Interface

Digital information can be stored in various types of electronic memories. ' 789 Patent col. 1, ll. 19-22. The chief form of memory used in a modern computer system is dynamic random access memory ("DRAM"). A DRAM stores data in a memory cell, and to prevent loss of the data the DRAM must periodically refresh the data by reading it from the cell and writing it back again. Id. at col. 1, ll. 31-34. Figure 1 shows a simple diagram of a prior art DRAM. The DRAM has an array with one or more banks of memory cells, an interface that routes signals coming into and going out of the DRAM, and interface pins that connect the interface to the bus. Id. at col. 1, ll. 35-42.

The interface communicates with the DRAM array through a multitude of connections. *See* id. at fig. 2. These connections include separate inputs for the row and column addresses, data, a write/read input signal, a row access strobe ("RAS"), a column access strobe ("CAS") signals, and a write enable ("WE") signal. Id. at col. 2, ll. 8-11. The row and column addresses identify the specific location in the memory array to be accessed. The write/read input signal is a control signal that indicates whether an operation is a read or a write. *See* id. at col. 2, ll. 4-6. The RAS and CAS signals are timing signals that indicate a row or column access operation. '789 patent at col. 2, ll. 3-4. Finally, during a write operation, the WE signal indicates whether a specific location in memory should be written to or not. Id. at col. 1, ll. 64-66.FN3

FN3. As this order later discusses, the parties dispute the exact nature of the "WE signal" disclosed by Messrs. Ware, Hampel, Stark and Griffin. To be clear, the court reproduces the exact text from the specification defining a "We signal:" "A WE signal indicates whether an associated byte is to be written or not during a write operation."

Using a WE signal to selectively write data can increase the performance of a DRAM. *See generally* id. at

col. 3, l. 60-col. 4, l. 18. For example, DRAMs sometimes implement error detection and correction schemes; one such scheme uses "parity bits." Id. at col. 4, ll. 9-11. A parity bit is a single bit that can be compared against the associated data to check for errors. Id. at col. 3, ll. 39-46. Calculating a parity bit for the associated data is time intensive, so the use of a WE signal increases speed by allowing the DRAM to avoid calculating the parity bit for data that need not be written. Id. at col. 4, ll. 14-18.

2. The Prior Art's Implementation of WE Signals

The inventors believed that prior art DRAM designs inefficiently used separate pins for the DRAM's many inputs. *See* id. at col. 2, ll. 12-14. The data, control signals and WE signals all required dedicated pins to connect to the bus. Id. at col. 2, ll. 7-11. The prior art contains a variety of schemes for multiplexing (i.e., transmitting different types of signals across the same pins at different points in time), which can reduce the number of pins required. Id. at col. 2, ll. 15-58. All of the prior art multiplexing schemes still required dedicated WE pins to receive the WE signals. Id. at col. 2, ll. 59-60. Furthermore, because these WE signals traveled a longer path than the data signals, the DRAM required a dedicated set of registers to store the incoming data signals as the DRAM awaited the arrival of the WE signal corresponding to the data. Id. at col. 2, ll. 60-63.

Rambus previously developed a method of multiplexing WE signals with data signals to reduce the number of pins required for the interface. Id. at col. 3, ll. 1-2. The operation begins by transmitting WE bits over eight "Bus-Data" lines in parallel. Id. at col. 3, ll. 3-6. The eight WE bits form a WE "word" 8 bits wide. Id. This particular scheme required sending eight WE words before transmitting data. Id. at col. 3, ll. 29-30.

Figure 8B illustrates Rambus's prior art method. Figure 8B is a graph showing the series of signals sent to the DRAM over time. Because the other figures in the Ware specification are similar, the court pauses to explain the format of the graph. The "vertical axis" represents times. It begins at the top of the graph and advances from an initial time at the top of the graph to the bottom. The graph measures time in units of clock cycles, with each hash mark on the vertical axis representing a full clock cycle. The "horizontal axis" consists of nine columns, each representing one data line connecting the bus to the DRAM interface. The lines are labeled Bus-Data 0 through 8. Each rectangular field on the graph represents a portion of information. A rectangle that is only one data line wide and only one half-clock cycle long represents a single bit of information (either a 0 or a 1). By its position on the graph, one can determine when that piece of information arrives at the DRAM and which data lines carry the information.

Rambus's prior art method for sending WE signals begins with the block labeled 981 above. Block 981 contains 64 bits of information, comprised of eight 8-bit "words" of WE information. Id. at col. 3, ll. 4-6. As shown, this block of WE information is sent over bus data lines 0 through 7 while bus data line 8 remains idle. Id . The arrows connect each WE bit to its corresponding byte of data. For example, the bit on data line 0 sent on the first half-clock cycle (i.e., the top right rectangle) indicates whether data byte 1000 should be written to memory or not. Id. at col. 3, ll. 18-21. Likewise, bit 1 indicates whether data byte 1001 should be written to memory or not. Id. Each 8-bit WE word conveys the WE information for eight data bytes, or a data block. Consequently, the first WE word, represented by the first row in figure 8B, contains all of the

WE information for data block 0. Id. at col. 3, ll. 17-18.

This prior art method transmits both WE signals and data signals over the bus data lines, that is, it multiplexes the WE and data signals. Using this method eliminates the need for a dedicated WE pin. *See generally* id. at col. 3, ll. 2-25. This advantageously reduces the number of pins on the DRAM, but requires the DRAM to temporarily store 64 bits of WE information while waiting for the WE bits' corresponding data words to arrive. Id. at col. 3, ll. 26-28. This method also suffers from having to interrupt data transmission after every eight blocks of data to send another eight words of WE information. Id. at col. 3, ll. 28-30.

3. The Ware Specification's Embodiments for Implementing WE Signals

The Ware patents disclose various ways of transmitting write enable information to a DRAM. Id. at col. 1, ll. 14-16. Some of the embodiments reduce the need to store WE bits prior to transmitting data. Id. at col. 5, ll. 46-49. Other embodiments multiplex the WE signals with data and error correction signals to reduce the number of pins needed for the DRAM interface. Id. at col. 5, ll. 49-52.

Figure 12A illustrates an embodiment that allows for multiplexing data and WE signals.FN4 *See* id. at col. 8, ll. 35-38. Unlike the Rambus prior art, it also uses a serial stream of WE bits that prevents the data transmission from having to be interrupted by the need to transmit additional WE information. The embodiment in Figure 12A uses a single pin for receiving WE signals, labeled 505 or "WE/Data." Id. at col. 7, ll. 9-10. The WE/Data pin appears as the leftmost column in the figure.

FN4. The court added the arrows that appear in Figure 12A to mirror the convention used in Figure 8B.

The first block of WE information is labeled 820. It is one bit wide and eight bits long, and it precedes the transmission of the data. Id. at col. 7, ll. 13-14; col. 7, ll 26-27. As shown by the vertical time axis, this transmission of the first WE block takes four complete clock cycles. While this first block of WE information is being transferred, the other inputs (bus data lines 0 through 7) cannot be used. Id. at col. 7, ll. 42-44. This first WE block contains the WE information for the data block labeled 711, whose transmission only begins once the entire WE block has arrived. Id. at col. 7, ll. 31-33.

While the first data block (711) is being transmitted, the DRAM also receives the next block of WE information, labeled 821. Id. at col. 7, ll. 33-35. This second WE block provides the WE information for the following data block, labeled 712. Id. This second WE block begins the "serial stream" of WE information that enables the DRAM to receive an uninterrupted amount of data because while the second data block is being received, the DRAM also receives the third WE block *See* id. at col. 8, ll. 39-43. The data transmission can continue in this fashion and never require interrupting for transmission of additional WE information.

Figure 13A represents an embodiment that blends the serial stream of WE bits from Figure 12A's

embodiment with the parallel transfer of WE bits seen in the prior art shown in Figure 8B. It begins with a parallel transfer of an eight-bit WE word (labeled 504) over bus data lines 0 through 7. *See* id. at col. 9, ll. 5-7, 39-40. The eight-bit WE word contains the same amount of WE information as the eight-bit WE block that started the sequence shown in Figure 12A. However, because Figure 13A's first WE word uses eight bus lines instead of one, it can be transmitted in a single half clock cycle, unlike the four complete clock cycles required to begin the data transmission shown in Figure 12A. *See* id. at col. 10, ll. 16-19. The specification dubs this a "quick start" because it allows data transmission to begin three and a half clock cycles earlier than otherwise. Id. at col. 10, l. 25.

Once the DRAM has received this first WE word (which the specification defines as a "WE mask"), the DRAM can begin receiving the corresponding data block (labeled 310).FN5 While the DRAM receives the first data block over bus data lines 0 through 7, it begins receiving a serial stream of WE bits on the pin labeled WE/Data (on the leftmost side of the graph). This is the same pin that was used for transmitting WE information in the Figure 12A embodiment. Id. at col. 9, ll 41-42. This serial stream of WE bits functions like the serial stream in Figure 12A and allows for an unlimited transfer of data. Id. at col. 10, ll. 25-29.

FN5. The court again added the arrows to Figure 13A to follow Figure 8B's convention of illustrating which blocks of WE information correspond to which blocks of data information.

The embodiment of Figure 14 modifies the parallel/serial hybrid of Figure 13A. FN6 This embodiment uses the same eight-bit WE mask (labeled 3010) to provide an initial "quick start" like in figure 13A. Id. at col. 10, ll. 59-62. Unlike figure 13A, this embodiment does not use the WE/Data pin to transmit a serial stream of WE bits. Instead, the block of information labeled 604 contains error correction information for the concurrent data block (labeled 3011). Id. at col. 10, ll 56-58. This configuration allows for the DRAM to receive both a "quick start" of WE information related to a data block as well as error correction information. Id. at col. 11, ll. 1-2.

FN6. Figure 14 has also been altered to add arrows to demonstrate the relationship between the WE information, the error detection and correction information and the data information. The court used a fat arrow to show the connection between the error detection and data information.

Figure 15 represents another embodiment that modifies the basic parallel/serial hybrid embodiment of Figure 13A. In this embodiment, the "WE mask," i.e., the 8 bits of parallel WE information used to "quick start" the DRAM, is appended to a request packet (labeled 500). Id. at col. 11, ll. 15-23. This 10-bit wide packet is sent over Bus-Data pins 0 through 7 as well as the WE/Data pin (505) and a bus control pin (499). Id. at

col. 11, ll. 27-31. Within the packet, the last word is the WE mask. Id. at col. 11, ll. 32-33.

The only difference between this embodiment and Figure 13A is that it integrates the teaching of Figure 13A into a packet-based protocol. This protocol is discussed extensively in the court's claim construction order addressing the other patents-in-suit. Rambus Inc. v. Hynix Semiconductor Inc., 2008 WL 2754805, *5-*6, *22-*27 (N.D.Cal.2008).

All four of these embodiments share a few features worth noting. First, they do not require a dedicated WE pin because the embodiments all employ some degree of multiplexing. '897 patent, col. 11, ll. 66-67. More importantly, these embodiments greatly reduce the amount of temporary storage needed on the DRAM. *See* id ., col. 12, ll. 2-9. In each of the embodiments, the arrival of the WE information precedes the arrival of the data information. This negates the need for registers to store the data information that plagued the prior art. *See* id. at col. 2, ll. 60-63. Furthermore, because one bit of WE information corresponds to a word of data information (normally, a word is 8 bits or one byte), the DRAM only needs enough space to store 1/8 of the information that it would have needed had it stored the data instead of the WE information. Finally, these embodiments never store more than eight bits of WE information (either the 8 bits from the serial start in Figure 12A, the 8-bit "quick start" in Figures 12A, 14 and 15, or any 8 bits received later from the serial stream). Id., col. 12, ll. 5-9. This represents a substantial reduction in the number of registers needed to store WE information over the prior art Rambus design demonstrated in Figure 8A. Id.

Figure 16A demonstrates another method of transmitting WE information, but it differs substantially from the embodiments displayed in Figures 12 through 15. The DRAM of Figure 16A receives WE bits only on the WE/Data pin (the leftmost pin, labeled 505). Id. at col. 12, ll. 20-21. It does not use the "WE mask" of Figures 13A, 14 and 15 to "quick start" the data transmission.

Furthermore, the Figure 16A does *not* supply WE information in advance of the corresponding data information. Id., col. 12, ll. 11-14. Instead, this embodiment uses a serial stream of WE bits that correspond to the block of data received by the DRAM at the same time. In Figure 16A, the blocks of WE information are labeled 6020-6023. Id. at col. 12, ll. 17-18. Each of these WE blocks conveys the WE information for the concurrent data block. Id. at col. 12, ll. 21-26. Figure 16B, displayed below, shows this relationship on a bit-by-bit basis. In Figure 16B, "WE 420" represents a single bit of WE information and it corresponds to data word 4110, a single byte of data.

Like the other embodiments, this configuration supports the unlimited transfer of data blocks and minimizes the amount of storage needed for holding data or WE information.

B. The Claims-In-Suit

Rambus has asserted that the Manufacturers infringe claim 13 of the '789 patent and claims 2 and 16 of the '897 patent. The claims-in-suit read as follows:

U.S. Patent No.; Claim	**Claim Language**[FN7]
6,493,789; 13	[A semiconductor memory device which includes sense amplifiers coupled to an array of memory cells, wherein the memory device comprises: a set of interface terminals to receive a plurality of control signals which specify that the memory device: receive a first set of data bits and a second set of data bits; precharge sense amplifiers used in writing the first set of data bits to the array; and precharge sense amplifiers used in writing the second set of data bits to the array; and a mask terminal to receive; a first mask bit during a first half of a clock cycle of an external clock signal, the first mask bit to indicate whether to write the first set of data bits to the array; and a second mask bit during a second half of the clock cycle of the external clock signal, the second mask bit to indicate whether to write the second set of data bits to the array] wherein: the first set of data bits is received during the first half of the clock cycle of the external clock signal; and
	the second set of data bits is received during the second half of the clock cycle of the external clock signal.

FN7. Bracketed text indicates that the claim is dependent on a prior claim. The bracketed text represents the prior claim's language that is incorporated in the dependent claim.

6,496,897; 2	[A method of operation in a semiconductor memory device, wherein the memory device receives an external clock signal and includes an array of memory cells, the method comprises: receiving, during a first half of a clock cycle of the external clock signal, a first data value and a first mask bit, wherein the first mask bit indicates whether to write the first data value to the array; and receiving during a second half of the clock cycle of the external clock signal, a second data value and a second mask bit, wherein the second mask bit indicates whether to write the second data value to the array]
	wherein the memory device is a dynamic random access memory device.
6,496,897; 16	[A synchronous semiconductor memory device, wherein the memory device receives an external clock signal and includes an array of memory cells, the memory device comprises: a pin to receive a first mask bit during a first half of a clock cycle of the external clock signal and to receive a second mask bit during a second half of the clock cycle of the external clock signal; and an interface to receive: a first data value with the first mask bit, wherein the first mask bit indicates whether to write the first data value to the array; and a second data value with the second mask bit, wherein the second mask bit indicates whether to write the second data value to the array] wherein the memory cells are dynamic random access memory cells.

II. CLAIM CONSTRUCTION

A. Claim Construction Legal Standard

The court begins its claim construction inquiry by considering the ordinary and customary meaning of the terms in the claims from the perspective of a person of ordinary skill in the art. *Phillips,* 415 F.3d at 1312-13. This ordinary meaning is influenced by the use of language in the asserted and unasserted claims in the patents. *Id*. at 1314-15. For example, the phrase "steel baffles" implies that a "baffle" need not be made of steel. *See id*. at 1314. More generally, the appearance of a limitation in a dependent claim creates a presumption that the independent claim lacks that limitation. *Id*. at 1315; *but see* Curtiss-Wright Flow Control Corp. v. Velan, Inc., 438 F.3d 1374, 1380-81 (Fed.Cir.2006) (discussing limits of claim differentiation).

This "objective baseline" of ordinary meaning is also formed in part by the patent specification's use of the claim language because a person of ordinary skill understands a claim's language in the context of the entire

patent. *Id*. at 1313. For example, the specification is often helpful in defining the scope of technical terms. *See id*. at 1315. The specification can also reveal a "special definition" of a claim term or demonstrate "an intentional disclaimer" or "disavowal" of claim scope. *Id*. at 1316. The specification's statutory role in determining a claim's validity justifies placing this heavy weight on it. *Id*. at 1315-16.

Similarly, the prosecution history of a patent can inform the proper construction of a patent's claims. *Id*. at 1317. It provides evidence of how both the Patent Office and the inventor understood the claims. *Id*. The prosecution history's back-and-forth nature often makes it unclear, however, and therefore it is rarely as helpful in construing a patent's claims as the claims themselves and the specification. *Id*. Still, the prosecution history can be invaluable for demonstrating the inventor's understanding of the claims and checking "whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id*.

Finally, a court may consider extrinsic evidence like inventor and expert testimony, dictionaries, and treatises. *Id*. at 1318. Such evidence can be helpful, but courts must be mindful that it is not necessarily created contemporaneously with the patent application and that the litigation context can produce biased evidence. *Id*. Accordingly, extrinsic evidence is rarely more probative of the proper construction of the claims than the intrinsic record, *id*. at 1319, but extrinsic evidence is particularly helpful "[w]hen the intrinsic evidence is silent as to the plain meaning of a term." Helmsderfer v. Bobrick Washroom Equipment, Inc., 527 F.3d 1379, 1381-83 (Fed.Cir.2008) (construing a claim term in light of three dictionary definitions); *see also Phillips,* 415 F.3d at 1322-23. Nonetheless, to avoid "the risk of systematic overbreadth" the court begins its inquiry focused "on how the patentee used the claim term in the claims, specification, and prosecution history, rather than starting with a broad definition and whittling it down." *Phillips,* 415 F.3d at 1321.

All four sources of evidence discussed above have their advantages and drawbacks and varying amounts of persuasive force. There is no "rigid algorithm" or "sequence of steps" which the court must follow in considering these sources of evidence. *Id*. at 1324. All that matters "is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law." *Id*.

B. "Mask Bit"

All three claims-in-suit include limitations reciting the use of a "mask bit." The parties' dispute turns on the meaning of "mask" in the phrase "mask bit." Rambus argues that "mask" refers to the act of masking a location in memory to prevent writing data there. To Rambus, a mask bit is identical to the WE bits discussed in the specification because both determine whether a data word should be "masked," or not written to memory. The Manufacturers argue that "mask" refers to a collection of eight WE bits transferred in parallel to "quick start" the data transfer. This collection of WE bits forms a "mask" that determines which portions of a subsequent data block should be written to memory. The parties' constructions appear below:

Claim term:	**Rambus's construction:**	**The Manufacturers' Construction:**
"mask bit"	A binary digit indicating whether to write data.	One of eight bits in a write-enable word.

The Manufacturers base their argument on the specification's use of the phrase "WE mask," which is the

only context in which the written description expressly uses the word "mask." As discussed above, the Figure 13A embodiment is the first embodiment to use a "WE mask." *See* '789 patent, col. 9, ll. 5-25. As described, the Figure 13A embodiment uses "initial write enable signals sent in parallel and subsequent write enable signals sent serially." Id. at col. 9, ll. 5-7. The written description refers to this initial transmission of WE signals in parallel as a "WE mask." Id. at col. 9, ll. 8-11. The WE mask of Figure 13A is "8 bits wide and one word long." Id. Referring to Figure 13A, the WE mask is the narrow rectangle toward the top of the figure labeled 504. To recap, "one advantage of starting write operations with the WE mask 504 is that the eight parallel WE bits of WE mask 504 are received by the DRAM in only one-half of a clock cycle." Id. at col. 10, ll. 16-19. This permits the "quick start" of the write operation. Id. at col. 10, ll. 25-29. But significantly, after the WE mask has been received, the Figure 13A embodiment switches to a serial stream of WE bits and "there is no requirement that the parallel WE mask 504 be sent again to enable writes." Id. at col. 10, ll. 29-30. This is the case because "the serial stream of WE bits allows the data words to keep being written to the DRAM." Id. at col. 10, ll. 31-33.

The Manufacturers argue that this consistent usage of the phrase "WE mask" would inform the person of ordinary skill's understanding of the phrase "mask bit" in the claims. Because a "WE mask" is routinely referred to as an 8-bit write enable word, the Manufacturers propose that a "mask bit" is "one of eight bits in a write-enable word."

While the Manufacturers' proposed construction is compelling when only the written description is considered, it cannot be reconciled with the language of the claims, and therefore must be rejected. All three claims include limitations that require a DRAM to receive a "first mask bit" during the first half of clock cycle and a "second mask bit" during the second half of a clock cycle. In all of the embodiments that use a WE mask (Figures 13A, 14 and 15), the DRAM receives the entire WE mask in the first half of a clock cycle. While it is conceivable that the DRAM could receive a second WE mask (for example, at the beginning of a new write operation many clock cycles later), the disclosed embodiments all switch from using a WE mask to "quick start" the write operation to a serial stream of WE bits to sustain the data transmission. If the court adopted the Manufacturers' proposed construction, none of the three asserted claims would read on the three embodiments that use a WE mask. The reason is that none of the embodiments receives a "second mask bit" on a second half clock cycle as the Manufacturers construe "mask bit." The embodiments do not receive a second WE mask; they instead receive the serial stream of WE bits on the WE/Data pin. Indeed, the parties confirmed that the Manufacturers' construction of "mask bit" would prevent claim 13 of the '789 patent from reading on the Figure 13A embodiment. *See* Claim Construction Hrg. Tr. 475:23-478:2 (Jun. 5, 2008).

Proper claim construction rarely results in construing a claim such that it does not cover a preferred embodiment. "Such an interpretation is rarely, if ever, correct and would require highly persuasive evidentiary support." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed.Cir.1996). Indeed, construing claims to read out preferred embodiments appears to be the "third rail" of claim construction. *See, e.g.,* Oatey Co. v. IPS Corp., 514 F.3d 1271, 1277 (Fed.Cir.2008) (reversing claim construction that read out a preferred embodiment), MBO Laboratories, Inc. v. Becton, Dickinson & Co., 474 F.3d 1323, 1333 (Fed.Cir.2007) (same); *On-* Line Tech. v. Bodenseewerk Perkin-Elmer, 386 F.3d 1133, 1138-39 (Fed.Cir.2004) (same); Burke, Inc. v. Bruno Independent Living Aids, Inc., 183 F.3d 1334, 1341 (Fed.Cir.1999) (same).

The Federal Circuit recently summarized the line of cases addressing constructions that read out disclosed embodiments and concluded that the "highly persuasive evidentiary support" required normally consists of

disclaimers in the specification or the prosecution history. Oatey, 514 F.3d at 1276-77, *see e.g.,* Elekta Instrument S.A. v. O.U.R. Scientific Int'l, Inc., 214 F.3d 1302 (Fed.Cir.2000) (affirming claim construction excluding preferred embodiment based on unambiguous prosecution disclaimer). Another recent case pointed out the importance of considering whether or not other claims in a patent might read on the allegedly excluded embodiment, and in affirming a claim construction that excluded an embodiment, the court pointed out that certain other claims might embrace it. Helmsderfer v. Bobrick Washroom Equipment, Inc., 527 F.3d 1379, 1383 (Fed.Cir.2008).

The Manufacturers fail to provide the evidentiary support required to accept their proposed claim construction. At most, the Manufacturers provide evidence from the prosecution history that the original Ware patent application's claims did not use the phrase "mask bit," but did use the phrases "serial sequence of write enable signals" and "serial sequence of write enable bits." The Manufacturers fail to explain why Rambus made any changes to the patent applications, and they do not explain why this evidence compels interpreting "mask bit" as a bit within a parallel transmission of WE signals, but not a serial transmission of WE signals. As noted in *Phillips,* the prosecution history "often lacks the clarity of the specification and thus is less useful for claim construction purposes." 415 F.3d at 1317. Here, the Manufacturers have failed to do anything but point out that Rambus has previously used different phrases to claim its inventions. This is far from the "highly persuasive evidentiary support" required to adopt the Manufacturers' proffered construction. Nor can the Manufacturers point to any other embodiment that the claims-in-suit might cover. None of the disclosed embodiments (Figures 12A, 13A, 14, 15 and 16A) transmits two WE masks in succession.

The parties also submit two dictionaries that bear on this dispute. The *1993 IEEE Dictionary* defines "mask" as "a pattern of characters that is used to control the retention or elimination of portions of another pattern of characters." *See* Murphy Decl. para. 218. The *Microsoft Press Computer Dictionary* (1991) defines a "mask bit" as "a given bit within a mask whose function is to screen out or let through the corresponding bit in a data value." *Id.* At first glance, these definitions might appear to support the Manufacturers' argument because each definition emphasizes that a "mask" is a group of characters. However, the definitions also lend some support to Rambus's proposed construction because each definition emphasizes the mask's function in determining how another bit of data is processed. Further, a person of ordinary skill with the understanding of these definitions would encounter the problem discussed above, namely, that the construction of the term "mask bit" proposed by the Manufacturers, when read in the context of the three claims-in-suit, corresponds to nothing discussed in the specification.

This is not to say that Rambus's proposed construction is free of difficulties. To begin, Rambus's construction of "mask bit" is synonymous with the specification's definition of "WE bit" or "WE signal." Rambus argues that a mask bit is a "binary digit indicating whether to write data," while in the specification, Rambus noted that a WE signal "indicates whether an associated byte is to be written or not during a write operation." *See, e.g.,* Claim Construction Hrg. Tr. 377:3-378:15 (Jun. 5, 2008) (Mr. Detre urging that a "mask bit" and "write enable signal" are synonymous).

Yet in a predecessor patent, Rambus claimed a method involving a first and second mask bit, and then in a dependent claim added the further limitation that "the first mask bit is a first write enable bit and the second mask bit is a second write enable bit." *See* U.S. Patent No. 6,266,737, col. 13, l. 62-col. 14, l. 4 (claims 1 and 2). Pursuant to the doctrine of claim differentiation, this prior usage suggests that Rambus understood "mask bits" to be distinct from "WE bits," though it now contends that they are identical. On the other hand, this does not support the Manufacturers' proposed construction of "mask bit" because the '737 patent's

claims still require both a first and second mask bit sent at different times. As discussed, the Manufacturers' construction cannot be reconciled with any of the embodiments set forth in the patent. In the end, an attempt to draw conclusions from claim differentiation of claims 1 and 2 of the '737 patent appear to be unhelpful and demonstrates a difficulty in some cases of applying the doctrine of claim differentiation. *Compare with* Rambus Inc. v. Hynix Semiconductor Inc., 2008 WL 2754805, *22-*24 (N.D.Cal. Jul. 10, 2008).

That aside, Rambus's proposed construction of the claims-at-issue accords with the disclosed embodiments, specifically Figure 16A. Figure 16A discloses a system for receiving WE bits contemporaneously with the data associated with each WE bit. It appears that the three claims-insuit attempt to claim this embodiment of the inventors' disclosure, and Rambus's construction accords with that. Nonetheless, the court cannot adopt Rambus's construction as proposed because it remains ambiguous. By defining a "mask bit" as a "binary digit indicating whether to write data," the construction blurs two distinct concepts. On the one hand, a DRAM receives a bit of information indicating whether an operation will be a read or a write operation. *See* '789 patent, col. 2, ll. 4-6. The Ware specification refers to this signal as a "W/R signal." Id. On the other hand, a DRAM can also receive a bit of information *during a write operation* indicating whether a particular piece of data should be written or not. The court's understanding of the specification and the claims indicate that Rambus's claims embrace the latter, but not the former. Nonetheless, Rambus's proposed construction of "mask bit"-"a binary digit indicating whether to write data"-could be misconstrued in the context of these claims to cover a "W/R signal" as well as the specification's "WE signal." Accordingly, the court opts to modify slightly Rambus's proposed construction. A "mask bit" is simply a "binary digit indicating whether to *mask* data involved in a write operation." This construction clarifies that the "mask" in "mask bit" refers to the action of masking data, and not the structure of a mask of data. It may also prevent future confusion about the scope of Rambus's claims.

C. "Mask Terminal" and "Pin"

Claim term:	**Rambus's construction:**	**The Manufacturers' Construction:**
"mask terminal"	A terminal that receives mask bits.	A pin that receives write-enable signals.

Turning to "mask terminal," the court agrees with the parties that the construction of a "mask terminal" turns on the construction of "mask bit." Rambus argues that a "mask terminal" is simply a terminal that receives mask bits. The Manufacturers argue that a "mask terminal" is a "pin that receives write-enable signals," but then point out that "each party defines [mask terminal] as a terminal that receives their version of a 'mask bit.' " Mfrs. Br. at 33-34. Apparently, the Manufacturers believe that a "terminal" and a "pin" are synonymous. Given the Manufacturers' response to the court's inquiry about their definition, Claim Construction Hrg. Tr. 398:5-13 (Jun. 5, 2008), the court sees no reason to introduce further ambiguity. The court is not convinced that it should narrow the meaning of "terminal" to only a "pin" and possibly exclude other terminal options. Accordingly, a "mask terminal" is simply a "terminal that receives mask bits."

D. "During a First/Second Half of a Clock Cycle of an External Clock Signal"

As discussed above, the DRAMs covered by the claims-in-suit receive a first mask bit and then receive a second mask bit. Each claim requires the DRAM to receive the first mask bit "during a first half of a clock cycle of the external clock signal" and the second mask bit "during a second half of a clock cycle of the

external clock signal." The parties' next disagree over the scope of this timing limitation. Their proposed constructions appear below:

Claim term:	Rambus's construction:	The Manufacturers' Construction:
"during a first/second half of a clock cycle of an external clock signal"	Phrase does not require separate construction, but is construed in view of the terms therein (see "clock cycle," "external clock signal"), plus plain meaning.	Only between two adjacent clock edges beginning with a rising edge of the clock signal and ending at the next falling edge of the clock signal or beginning with a falling edge of the clock signal and ending at the next rising edge.

The Ware specification says very little about clocking. *Compare with* Rambus Inc. v. Hynix Semiconductor Inc., 2008 WL 2754805 (N.D.Cal. Jul. 10, 2008) (construing Rambus's Farmwald/Horowitz patents's clocking terms). The only statement in the Ware specification regarding the invention occurs in the discussion of the Figure 12A embodiment. There, the inventors noted that "[f]or the embodiments of the invention, a single clock cycle has two phases, allowing two transfer operations within a single clock cycle" and that "[f]or alternative embodiments, other clocking schemes may be used." '789 Patent at col. 7, ll. 21-24.

Absent any help from the intrinsic evidence, the court turns to extrinsic evidence of how a person of ordinary skill in the art would understand "during a first half of a clock cycle." Helmsderfer, 527 F.3d at 1382. The Manufacturers' expert, Mr. McAlexander, states that "a clock cycle is measured between two consecutive rising (leading) edges of a clock signal." McAlexander Decl. para. 138. Mr. McAlexander concludes that this mandates the Manufacturers' proffered claim construction because that would be the understanding of person of ordinary skill in the art. *Id*. para.para. 139, 140. Mr. McAlexander cites no support for these statements. On the other hand, Rambus's expert, Mr. Murphy, states that the phrase requires no construction. Murphy Decl. para. 247. Mr. Murphy criticizes Mr. McAlexander's construction of the term as arbitrary, but also cites no support for what a person of ordinary skill would understand. The Federal Circuit has observed that "extrinsic evidence consisting of expert reports and testimony is generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence." *Phillips,* 415 F.3d at 1318. The court is concerned that the views of the experts suffer from such bias here, and therefore, it accords little weight to the opinion testimony of either.

This leaves the dictionaries. The most probative dictionary submitted is the *1996 IEEE Dictionary,* which defines "clock cycle" as "one period of the [clock] signal, beginning with the rising edge of the signal and ending on the following rising edge of the signal." This supports the Manufacturers' proposed construction of phrase "during the first half of a clock cycle." But absent the idealized square wave used to model a clock signal, the Manufacturers' construction is plagued by the practical question of how to measure "the beginning of the rising edge" of a clock signal. Would a person of ordinary skill understand that a "rising edge" begins when the voltage begins increasing? When the voltage crosses the midpoint from negative to positive?

Given the cursory briefing associated with this dispute, the court declines to construe to the phrase at the present time. As this phrase requires construction before the court may address the Manufacturers' motion for summary judgment of non-infringement, the court requests that the parties simultaneously submit a brief of up to 10 pages on this topic by August 1, 2008. Each side may submit up to 5 pages in reply one week later.FN8

FN8. The court recognizes that Rambus's final infringement contentions are due on August 1, 2008. The parties may stipulate to extend the deadline for final infringement contentions of the Ware patent claims affected by this unresolved dispute. If the parties cannot agree, they may submit a joint statement outlining their proposals for modifying the schedule.

E. "First/Second Mask Bit with a First/Second Data Bit"

Lastly, the parties disagree on the meaning of "with." Specifically, the parties dispute the degree of precision required for a DRAM to have received one signal "with" another. The Manufacturers argue that in the context of the claims "with" means "at the same time." Rambus argues that "with" means during the same first/second half of a clock cycle. The parties' constructions appear below:

Claim term:	Rambus's construction:	The Manufacturers' Construction:
"first/second data value with the first/second mask bit"	First/second data value is received during the first/second half of a clock cycle of the external clock signal.	The information is received at the interface at the same time as the mask bit.

Of the three claims, only claim 16 of the '897 patent uses the disputed phrasing. Claim 16 recites a synchronous semiconductor memory device. One of the limitations is "a pin to receive a first mask bit during a first half of a clock cycle of the external clock signal." The disputed limitation requires "an interface to receive ... a first data value with the first mask bit, wherein the first mask bit indicates whether to write the first data value to the array."

Throughout the Ware specification, time is measured in clock cycles and transfers occur within half-clock cycles. *See, e.g., supra,* Figs. 8B, 12A, 13A, 14, 15, 16A & 16B. The specification teaches that the appropriate margin of error for the invention is therefore less than one half of a clock cycle. But so long as the data value and the mask bit arrive within the same half clock cycle, the DRAM can perform the required operation. The Manufacturers' proposed construction could lead to mischief if interpreted by the lay jury to mean "simultaneously." While Rambus's proposed construction may represent too broad a margin of error for receiving a mask bit and a data value, the Manufacturers have not introduced any evidence to suggest this and made no argument to that effect. Accordingly, the court adopts Rambus's proposed construction of the phrase.

IV. NON-INFRINGEMENT

The Manufacturers have moved for summary judgment of non-infringement based on the court adopting their proposed construction of "mask bit." It has not, so the court denies that portion of the Manufacturers' motion for summary judgment as moot. The Manufacturers have also moved for summary judgment of non-infringement based on the court adopting their construction of "during a first half of a clock cycle." The court has deferred construing that phrase, and likewise defers ruling on that portion of the Manufacturers' motion for summary judgment of non-infringement.

V. INVALIDITY

The Manufacturers' motion for summary judgment of non-infringement includes a motion for summary

judgment of invalidity contingent on the court adopting Rambus's construction of the phrase "mask bit." The court has done so. The ruling on the motion for summary judgment will be in a separate order.

VI. ORDER

For the reasons set forth above, the court construes the claims as described. The Manufacturers' motion for summary judgment of non-infringement with respect to the "mask bit" claims is denied as moot. The court defers ruling on the Manufacturers' remaining motions for summary judgment.

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