United States District Court,
N.D. California.

HYNIX SEMICONDUCTOR INC,
Plaintiff.
v.
TOSHIBA CORPORATION, et al,
Defendants.
And Related Counterclaim,
And Related Counterclaims.

No. C-04-04708 VRW

Sept. 1, 2006.

Daniel J. Furniss, Theodore G. Brown, III, Anne M. Rogaski, Eric P. Jacobs, Susan M. Spaeth, Townsend and Townsend and Crew LLP, Palo Alto, CA, Keith L. Slenkovich, Kenneth L. Nissly, Susan G. Van Keulen, Thelen Reid & Priest LLP, San Jose, CA, Robert A. McFarlane, Townsend and Townsend and Crew LLP, San Francisco, CA, for Plaintiff.

Ronald Loh-Hwa Yin, Alan A. Limbach, Erin Overom Dungan, Mark Fowler, Vincent Lam, Dla Piper Rudnick Gray Cary U.S. LLP, East Palo Alto, CA, for Defendants.

ORDER

VAUGHN R. WALKER, **District Chief Judge.**

Plaintiff/counterdefendant Hynix Semiconductor, Inc ("Hynix") owns the eleven patents-in-suit, which relate to the design and manufacture of semiconductors. Defendant/ counterclaimant Toshiba Corporation seeks a judgment declaring that these patents are invalid and unenforceable or alternatively that Toshiba has not infringed any valid claims in these patents. Doc # 1 at 23-24; Doc # 25 at 16. Hynix denies these invalidity allegations and claims that Toshiba Corporation and various related entities (collectively, "Toshiba") have infringed the patents. Doc # 12 at 23.

On March 29, 2006, the court held a claim construction hearing pursuant to Markman v. Westview Instruments, Inc, 517 U.S. 370 (1996), for the disputed terms in four of these patents: United States Patent Nos 5,422,311 ("'311 patent"); 5,512,519 ("'519 patent"); 6,330,190 ("'190 patent") and 5,031,111, which was subsequently reexamined in Reexamination certificate 4297 ("'111 patent"). Based on the parties' submissions to the court and their arguments at the hearing, the court issues the following claim construction order. As the court writes principally for the parties, it will not discuss the details of the inventions or define terms well-known to those skilled in the art, except as is necessary to construe the patent claims.

I

The construction of patent claims is a question of law to be determined by the court. Id at 384. The goal of claim construction is "to interpret what the patentee meant by a particular term or phrase in a claim." Renishaw PLC v. Marposs SpA, 158 F3d 1243, 1249 (Fed Cir1998). In doing so, the court looks first to the claim itself:

The claims of the patent provide the concise formal definition of the invention. They are the numbered paragraphs which "particularly [point] out and distinctly [claim] the subject matter which the applicant regards as his invention." 35 USC s. 112. It is to these wordings that one must look to determine whether there has been infringement. Courts can neither broaden nor narrow the claims to give the patentee something different than what he has set forth. No matter how great the temptations of fairness or policy making, courts do not rework claims. They only interpret them.

EI Du Pont de Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 1433 (Fed Cir1988).

"The claims define the scope of the right to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim." Renishaw, 158 F3d at 1248. "The words used in the claim are viewed through the viewing glass of a person skilled in the art." Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc, 326 F3d 1215, 1220 (Fed Cir2003) (citing Tegal Corp v. Tokyo Electron Am, Inc, 257 F3d 1331, 1342 (Fed Cir2001)). "Absent a special and particular definition created by the patent applicant, terms in a claim are to be given their ordinary and accustomed meaning." York Prods, Inc v Central Tractor Farm & Family Ctr, 99 F3d 1568, 1572 (Fed Cir1996). The court may, if necessary, consult a variety of sources to determine the ordinary and customary meaning of a claim term, including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." Innova/Pure Water, Inc v. Safari Water, 381 F3d 1111, 1116 (Fed Cir2004).

The court begins its construction of claim terms by consulting intrinsic evidence of the meaning of disputed claim terms, which includes the claims, the specification and the prosecution history (if in evidence). Lacks Industries, Inc v McKechnie Vehicle Components USA, Inc, 322 F3d 1335, 1341 (Fed Cir2003) (citation omitted). "If upon examination of this intrinsic evidence the meaning of the claim language is sufficiently clear, resort to 'extrinsic' evidence * * * should not be necessary." Digital Biometrics, Inc, v. Identix, Inc, 149 F3d 1335, 1344 (Fed Cir1998). "[I]f after consideration of the intrinsic evidence, there remains doubt as to the exact meaning of the claim terms, consideration of extrinsic evidence may be necessary to determine the proper construction." *Id*. Although extrinsic evidence such as expert and inventor testimonies, dictionaries and learned treatises can shed useful light on the relevant art, extrinsic evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." Phillips v. AWH Corp, 415 F3d 1303, 1317 (Fed Cir2005) (quoting C R Bard, Inc. v. United States Surgical Corp, 388 F3d 858, 862 (Fed Cir2004)) (internal quotation marks omitted).

"[A] court may constrict the ordinary meaning of a claim term in at least one of four ways[:]" (1) "if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim in either the specification or prosecution history;" (2) "if the intrinsic evidence shows that the patentee distinguished [the] term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention;" (3) "if the term chosen by the patentee so deprives the claim of clarity as to require resort to the other intrinsic evidence for a definite meaning;" or (4)

"if the patentee phrased the claim in step- or means-plus-function format," then "a claim term will cover nothing more than the corresponding structure or step disclosed in the specification, as well as equivalents thereto * * *." CCS Fitness, Inc v. Brunswick Corp, 288 F3d 1359, 1366-67 (Fed Cir2002) (internal citations and quotation marks omitted).

Limitations from the specification, such as from a preferred embodiment, cannot be read into the claims unless expressly intended by the patentee. Teleflex, Inc v. Ficosa North Am Corp, 299 F3d 1313, 1326 (Fed Cir2002) ("The claims must be read in view of the specification, but limitations from the specification are not to be read into the claims."). And "a construction that excludes a preferred embodiment 'is rarely, if ever, correct.' " C R Bard, 388 F3d at 865 (citing Vitronics Corp v. Conceptronic, Inc, 90 F3d 1576, 1583 (Fed Cir1996)).

With these legal principles in mind, the court now construes the disputed claim language in the patents.

II. ***The*** '311 patent

The '311 patent issued on June 6, 1995, and discloses a method of fabricating conductive layers in a semiconductor device and decreasing the layers' resistivity. The patent addresses a basic problem of integrated circuit design: as the size of the conductive layers in a semiconductor device decreases, the device's resistivity increases, resulting in power dissipation and signal delay. Doc # 85 at 9.

1. "amorphous silicon film"

"Amorphous silicon film" appears in claims 1 and 6. Hynix contends this term means "a thin covering or coating of silicon that is devoid of long-range periodic structure." Doc # 85 (Hynix Br) at 12; Doc # 91 (Joint Cl Const), App 2 at 1. Toshiba instead construes the term as "[a] layer of silicon that is entirely non-crystalline and non-polycrystalline in form, formed in a temperature range insufficient to cause the formation of polysilicon ." Doc # 87 (Toshiba Br) at 3.

First, the specification fails to support Toshiba's proposed limitation mandating that the amorphous silicon film must be "formed in a temperature range insufficient to create polysilicon." Although the specification mentions temperature ranges at which an amorphous silicon film might be annealed and therefore turn into a polysilicon film, the specification never suggests that an amorphous silicon film can be formed only below these temperatures. In essence, Toshiba is asking the court to limit this term based solely on a disclosed embodiment, which is something the court cannot do. Phillips, 415 F3d at 1323. Moreover, Toshiba's proposed temperature limitation would tend to render superfluous dependent claims 3 and 8, which specify a particular temperature range at which an amorphous silicon film could be formed. See, e g, '311 patent at claim 3 (the "silicon film is deposited * * * at a temperature of 450-550 degrees Celsius"). Toshiba's proposed construction is in tension with the doctrine of claim differentiation, which "creates a presumption that each claim in a patent has a different scope." Free Motion Fitness, Inc v. Cybex Intl, 423 F3d 1343, 1351 (Fed Cir2005) (quoting Comark Communications, Inc v. Harris Corp, 156 F3d 1182, 1187 (Fed Cir1998)). Cf id ("[D]ependent claims limiting the claim to a single cable confirm that the independent claims may encompass more than one cable.").

Similarly, Toshiba's proposed limitation requiring the "amorphous silicon film" to have no structure at all, i e, to be "*entirely* non-crystalline and non-polycrystalline," is unduly restrictive. The patent consistently contrasts an "amorphous silicon film" with the "polysilicon film" that is created after the "amorphous silicon film" is annealed. See, e g, '311 patent at 1:61-65 ("[A]n in-situ phosphorus doped amorphous silicon film

is deposited on the substrate. The silicon film is then annealed to form a polysilicon film * * *."; id at 2:65-68 ("FIG 1B illustrates the formation of the polysilicon film 3a by annealing the silicon film 3 at a temperature above 800 degree Celsius * * *."); id at 3:60-63 ("FIG 2B illustrates the formation of a polysilicon film 3a by annealing the silicon film 3a at a low temperature of about 600 degrees Celsius under inert gas environment during a prolonged period * * *."). But the specification never suggests that an amorphous film necessarily lacks any structure. Common sense dictates that an amorphous silicon film, though certainly less structured than a polysilicon film, could have some small structural pockets. The treatise on which both parties rely supports such a construction. See Doc # 86, Ex G and Doc # 88, Ex H ("Solid matter exists in crystalline and amorphous forms. * * * *Amorphous* materials are devoid of long-range periodic structure.") (from Stanley Wolf & Richard Tauber, *Silicon Processing for the VLSI Era,* Vol 1-Process Technology at 1-2 (Lattice Press 1986).

Hence, because the specification contrasts "amorphous silicon film" from "polycrystalline" and "crystalline" films, the court construes an "amorphous silicon film" as a "a thin covering or coating of silicon that lacks sufficient structure to be crystalline or polycrystalline in form."

2. (a) "and then annealing said tungsten silicide film to form a polycide film and to form a silicon layer" and

(b) "silicon layer at the boundary between said tungsten silicide film and said polysilicon film"

For purposes of this subsection, any reference to "first term" is to term 2(a) above and any reference to "second term" is to term 2(b) above. These two terms together comprise the bulk of the third clause of claim 1 and the fourth clause of claim 6; the only difference between the two clauses is that the latter clause has the word "reduced" appearing before "polysilicon film." Claim 1's third clause reads in full (with the terms to be construed emphasized):

depositing a tungsten silicide layer on said polysilicon film *and then annealing said tungsten silicide film to form a polycide film and to form a silicon layer at the boundary between said tungsten silicide film and said polysilicon film*

Although the parties briefed these terms separately, the court examines them together because each term provides guidance as to the other term's meaning.

Hynix proposes that "silicon layer" means "a region or regions of silicon" and that the remainder of the first term need not be construed by the court. Doc # 85 at 12-13. Alternatively, Hynix asserts that: (1) "and then" means "after that;" (2) "annealing" means "heat treat[ing];" (3) "tungsten silicide film" means "a thin covering or coating which comprises tungsten and silicon atoms in a variety of possible stoichiometric ratios" and (4) "polycide film" means "a multilayer structure comprising a low resistance material such as a refactory [sic] metal silicide (e g, tungsten silicide or titanium silicide) overlaying a layer of doped polycrystalline silicon." Joint Cl Const, App 2 at 4. For the second term, Hynix proposes that (1) "silicon layer at the boundary between said tungsten silicide film and said polysilicon film" means "a region or regions of silicon formed at the boundary between said tungsten silicide film and said polysilicon film" and (2) "polysilicon film" means "a thin covering or coating of polycrystalline silicon, i e, solid silicon composed of small single crystal regions." Id at 8.

Toshiba contends the first term means "[a] single thickness of a homogeneous silicon-only material and

polycide film comprising the composite film of a tungsten silicide film and a polysilicon film are both formed after the composite film is annealed, and before the polycide layer is patterned, wherein the silicon-only material is formed by the transfer of silicon from the tungsten silicide film." Id at 4. Toshiba proposes that the second term means "[a] single thickness of a homogeneous silicon-only material is located at the lateral extent of a plane separating the tungsten silicide film and the polysilicon film, which defines where one film begins and the other film ends, wherein the silicon-only material is transferred from the tungsten silicide film decreasing the silicon in the tungsten silicide film." Id at 8. Toshiba further defines "polysilicon film" as "a layer of silicon having an aggregate of more than one island of crystalline grains."

The court begins pruning this thicket of terms by observing that both parties apparently agree that "and then" means "after that" and "annealing" means "heat treat[ing]." The court now turns to the disputed terms.

a. "polysilicon film"

As noted previously, the specification consistently contrasts "polysilicon" from "amorphous silicon." See *supra* section II(1). Although the term "polysilicon film" is never explicitly defined in the specification, it is evident based on the usage of "polysilicon film" throughout the specification that the patentee assumed that one having ordinary skill in the art would be familiar with the meaning of this straightforward term. See, e g, '311 patent at 1:7-11 ("Generally, a conductor layer in a semiconductor device is formed by utilizing a polycide having a low resistivity. In order to make the polycide, a polysilicon film is formed on a silicon substrate * * *."); id at 1:14-17 ("[A]s semiconductor device integration is increased, the thickness of the polysilicon film must be decreased."); id at 1:24-26 ("[T]he major factors in determining the resistivity of the polysilicon film are its impurity density, thickness and the grain size of the film * * *."). Because the patent does not appear to have used "polysilicon film" outside its conventional meaning and because that meaning is sufficiently clear to one having ordinary skill in the art, the court declines presently to construe this term.

b. "silicon layer"

First, the relevant claim language supports Toshiba's construction. The relevant clause in which this term appears states: "*and then annealing* said tungsten silicide film *to form a polycide film and to form a silicon layer* at the boundary between said tungsten silicide film and said polysilicon film." Accordingly, the claim itself states that the act of annealing the tungsten silicide film is what creates the silicon layer, at least suggesting that the silicon in that layer comes from the tungsten silicide film.

This specification also supports Toshiba's construction by consistently noting that the silicon layer is formed only by silicon leaving the tungsten silicide film when that film is annealed to the polycide film. Although a court generally should not import limitations from the specification based on disclosed embodiments, "where the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims." Alloc, Inc v. ITC, 342 F3d 1361, 1370 (Fed Cir2003) (internal citations omitted). Here, the specification makes clear that "the very character of the invention," id, requires the silicon layer to be formed only from the tungsten silicide film rather than any other possible source. See, e g, '311 patent at abstract ("[T]he silicon in the tungsten silicide film is transferred to the boundary between the tungsten silicide film and the polysilicon film to increase the adhesion properties therebetween."); id at 3:28-36 ("FIG 1D illustrates the formation of a silicon layer 5 at the boundary between the tungsten silicide film 4 and the reduced polysilicon film 3b. The silicon layer 5 is formed by annealing the tungsten silicide film 4 and the reduced polysilicon film 3b * * *. The silicon in the tungsten silicide film 4 is transferred to the boundary between the tungsten silicide film 4 and the reduced

polysilicon film 3b having the large grain size."); id at 4:4-11 (same for FIG 2D).

Still, Toshiba's proposed construction is unduly complicated and restrictive. For example, Toshiba adds a timing limitation, requiring the silicon layer to be "formed after the composite film is annealed, and before the polycide layer is patterned." This limitation is unnecessary, given that the claims themselves specify the order in which these steps must occur. For example, claim 1's use of antecedent basis makes clear that step b must occur before step c. See '311 patent at claim 1 (step b: "annealing said silicon film to form a polysilicon film * * *;" step c: "depositing a tungsten silicide film on said polysilicon film and then annealing said tungsten silicide film * * * to form a silicon layer * * * "). Similarly, step c by necessity occurs before step d (step d: "patterning said polycide film * * * ").

Accordingly, the court adopts a blended version of the parties' constructions: "a region or regions of silicon formed by the transfer of silicon from the tungsten silicide film."

c. "tungsten silicide film"

Although the specification does not explicitly define what constitutes a "tungsten silicide film," the specification provides various details in particular embodiments that would enable one having ordinary skill in the art to build such a film. See, e g, '311 patent at id at 3:7-10 ("A tungsten silicide film 4 having a W-Six structure is formed on the reduced polysilicon film 3b after impurities generated by the annealing of the polysilicon film 3a have been removed."); see id at 3:67-4:3 ("FIG 2C illustrates the formation of a tungsten silicide film 4 on the polysilicon film 3a after impurities, generated by the annealing of the polysilicon film 3a at a low temperature during a long period of time in a solid state, have been removed."); id at 2:25-28 ("[T]he polysilicon film and tungsten silicide film are annealed at a temperature of 800-1000 degrees Celsius to form the silicon layer at the boundary therebetween."). In light of the specification, the meaning of this term would be known to one having ordinary skill in the art. Accordingly, the court presently declines to construe this term.

d. "polycide film"

Because "polycide film" is already clearly defined by the claim, the court declines to construe this term. See '311 patent at 4:52-55 ("the polycide film is formed by depositing a tungsten silicide film on the polysilicon layer and then annealing the two").

III. ***The*** '519 patent

The '519 patent, which issued on April 30, 1996, discloses a method of forming a silicon insulating layer that independently supplies and controls the flow rate of nitrous oxide and oxygen gases.

1. "supplying and exposing the silicon surface to an O2-containing gas"

Hynix proposes the term should be construed to mean "providing a gas that contains O2 and subjecting the silicon surface to said gas." Doc # 85 at 16. Toshiba contends the claim should instead be construed as "providing a gas that contains O2 and subjecting the uncovered surface of silicon to said gas." Doc # 87 at 9.

Although the parties appear to agree that "supplying" should be construed to mean "providing a gas that contains O2," the parties dispute whether the "silicon layer" must be uncovered. Toshiba argues that the claim language necessarily implies that the silicon surface must be uncovered, because otherwise the surface

could not be exposed to the oxygen gas. Doc # 87 at 9. Hynix argues that Toshiba's proposed construction of "silicon layer" cannot be squared with Toshiba's proposed use of "exposing:" "If the claim term 'exposing' required the surface being exposed to be uncovered as Toshiba seeks to require in the first step, it would, of course not be possible to 'expose' the silicon surface after it is covered by an oxide layer." Doc # 92 at 6.

Toshiba's argument is supported by the patent's use of "silicon surface." The patent distinguishes the "silicon surface" that is exposed to an oxygen gas to form an oxide layer in claim 12 from the silicon layer that is covered by an oxide layer in claim 15. See '519 patent at 4:60-61 ("exposing the silicon surface to an O2 containing gas to form an oxide layer on the silicon surface") (emphasis added); id at 5:10-11 ("wherein the silicon surface having an oxide layer is exposed to an NO-containing gas at a second temperature") (emphasis added). Hynix's argument ignores that the claim does not assert that the silicon layer is the only material exposed to the gas after the oxide layer has been formed; rather "the silicon layer having an oxide layer" is exposed. By specifying when the silicon surface is covered by another material, the claims imply that the term "silicon layer" is generally uncovered unless otherwise stated. Compare Phillips, 415 F3d at 1314 (use of term "steel baffles" strongly implies that not all baffles are made of steel).

Accordingly, the court adopts Toshiba's construction and defines "supplying and exposing the silicon surface to an O2-containing gas" to mean "providing a gas that contains O2 and subjecting the uncovered surface of silicon to said gas."

2. "a gas containing essentially NO"

At the claim construction hearing, the parties appeared to agree that this term should be construed as "a gas predominantly composed of NO." The court adopts this reasonable construction.

3. "supply of NO and O2 containing gases is regulated independently"

Hynix proposes this term should be construed to mean "supply of NO-and O2-containing gases is separately controlled." Doc # 85 at 18. Toshiba asks the term be construed as "the flow of each of the gases containing NO and O2 is controlled not dependent on the other." Doc # 87 at 10. The parties appear to agree that "regulating" means "controlling" but dispute the meaning of "independently."

Hynix's proposed construction is undercut by both the prosecution history and the term's use in the patent. The claim was amended to insert the term "independently" prior to "regulating" in order to circumvent the prior art. See Office Action Dated 4/12/95 at p 3, Doc # 88 Ex N. The examiner explained:

The art has recognized the need for incorporating nitrogen into a Si/SiO2 interface[.] * * * Therefore it would have been obvious for one skilled in the art to independently control the flow rates of active reactants * * * The examiner will withdraw the rejection if "independently" is inserted before regulating.

Id.

Again, Hynix's proposed construction appears to be an attempt to recover ground it surrendered during claim construction because the language "separately control[ing]" the supply rate of the NO-and O2 gases is analogous to "independently control[ing" the flow rate of these active reactants, which is an action that the examiner explicitly stated would be obvious to one skilled in the art.

Moreover, the specification's use of the term further illuminates the error of Hynix's proposed construction.

First, the specification states that the gases are regulated at different times, or steps, of the process. See '519 patent at 2:56-60 ("[T]he flow rate of the O2 gas is highly regulated at the beginning of the oxidation process, and then the flow rate of the NO gas is highly regulated at the end of the oxidation process."). Further, the specification recites the independent purpose of each gas. See '519 patent at 2:52-55 ("To obtain a thicker oxide layer, the flow rate is regulated to flow the O2 at a higher rate. In order to increase the amount of nitrogen included in the oxide lawyer, the flow rate of the NO gas is regulated to flow at a higher rate."). Accordingly, the specification clarifies that the gases are not just "separately controlled;" rather, their regulation occurs at different times and for different purposes. Hynix's proposed construction fails to capture this nuance.

By contrast, Toshiba's proposal comports with the intrinsic evidence. While the specification makes clear the gases are "separately" controlled, the disclosed preferred embodiments emphasize the gases have different functions, and should be controlled at different steps, which suggest the gases should be regulated "not dependent" on the other. The ordinary and accustomed meaning of "independent" is "not dependent" and the specification makes clear that the drafter did not intend to be his own lexicographer but rather to adopt this customary meaning. Accordingly, the court defines the term to mean "the flow of each gases containing NO and O2 is controlled not dependent on the other."

IV. *The* '190 patent

The '190 patent, which issued on December 11, 2001, discloses a flash memory structure that is formed in a silicon substrate, which permits the use of lower voltages in programming and erasing data than employed by the prior art.

1. "The difference between the first positive potential and second positive potential is no more than about 1 volt."

The term appears in claim 13 of the patent. Hynix argues the term need not be construed, but in the alternative contends that the term means "any difference between the positive potential applied to the source is less than or equal to 1 volt." Doc # 85 at 31. Toshiba asserts the term should be construed to mean "the first potential and second potential are different resulting in a difference which does not exceed one volt." Doc # 87 at 15. The parties apparently contest whether there must be a difference in voltage between the positive potential applied to the source and the positive potential applied to the second well region.

a. "The difference"

Toshiba contends the term "difference between the first and second positive potential is no more than about one volt" necessarily implies that there must be a difference between the first and second positive potentials. ' 190 patent at 14:37-38; Doc # 87 at 14. But this argument misses the point. Simply because the difference between these potentials can be "no more than about 1 volt," does not mean the first and second potentials cannot be the same. Indeed, a difference of zero is certainly contemplated by this language.

Moreover, the preferred embodiments in the specification refute Toshiba's assertion. Table 1 discloses a range of voltages that can be separately applied to the source and the second well in order to perform the erase operation. ' 190 patent 7 :1-20. The parties agree that "Erase-2" is an illustration of the erase operation of claim 13. Doc # 87 at 14; Doc # 92 at 18. Because the possible ranges for these two potentials (3.0 to 6.5 for the source and 2.0 to 6.0 for the well) overlap, the specification explicitly provides that these two separately applied voltages could be the same.

b. "no more than about one volt."

Hynix asserts this term should be construed as "less than or equal to 1 volt." Hynix asserts the patentees demonstrated their intent to be their own lexicographer by characterizing this limitation as "no more than 1 volt" during prosecution. Doc # 85 at 31. In the remarks section of its application to amend the '519 patent, the inventor states:

Sato et al discloses applying 3 volts to the P-well and 8 volts to the source. [ ] Sato discloses an erase method that maintains the potential difference of 5 volts between the P-well and source to prevent the need for raising the junction breakdown voltage[ ]. Therefore, Sato et al teaches away from the invention as recited in claim 8, reciting the potential difference between the first positive potential and second positive potential being no more than 1 volt.

Doc # 93, Ex EE at 7.

Contrary to this explanation, however, the amended claim uses the term "no more than about 1 volt" as it appears in the issued patent. Because "[t]he claim construction inquiry * * * begins and ends in all cases with the actual words of the claim," Renishaw, 158 F3d at 1248, applicants' explanation of the amendment in the remarks section is less important than the actual language of the amended claim itself. Moreover, given that applicants were trying to distinguish the claim limitation from prior art disclosing a potential voltage difference of 5 volts, it appears that their explanation simply includes a typographical, rather than a deliberate, omission. By its very terms "no more than about one volt" denotes a range of variation both slightly less than and slightly greater than one volt.

Accordingly, the court adopts a hybrid construction: "the difference between the first positive potential and second positive potential is no more than about one volt" means "any difference between the first positive potential and the second positive potential does not exceed about 1 volt."

2. "An erase operation"

Hynix contends the term, which appears in claim 13, refers to "the removal of charge carriers from the floating gate of the memory cell." Doc # 85 at 30. Toshiba proposes the term should be construed as "an operation to erase a floating gate nonvolatile memory cell wherein different voltages are applied to the source (or the drain) and to the channel of the cell to create a voltage difference therebetween." Doc # 87 at 14. The parties agree the memory cell at issue is the floating gate, though Toshiba's construction uses the term "floating gate non-volatile memory cell" while Hynix merely uses "the floating gate of the memory cell." Again, the point of contention between the parties is whether there must be a difference in voltage between the two positive potentials. Additionally, Toshiba uses the term "channel" interchangeably with "well region," a usage that Hynix does not appear to dispute. See Doc # 85 at 14; Doc # 92.

In pertinent part, claim 13 reads:

To perform an erase operation on a selected memory cell from the plurality of memory cells, a negative potential is applied to the control gate of the selected memory cell, a first positive potential is applied to the source of the selected memory cell, and a second positive potential is applied to the second well region of the selected memory cell, wherein the difference between the first positive potential and second positive potential is no more than about 1 volt

'190 patent at 14:29-39.

Toshiba contends its construction is proper because (1) two potentials are separately applied to the source and well region and (2) there must be a difference between the two voltages applied. Doc # 85 at 14. As with the previous term, the court once again rejects Toshiba's contention that the two applied potentials must be different; the claim language does not preclude these voltages from being the same.

Moreover, Toshiba's proposed construction is redundant with the rest of claim 13. Because claim 13 itself specifies that the erase operation is performed by applying a first positive potential to the source region and a second positive potential to the well region, it makes little sense to construe "an erase operation" as necessarily including these limitations. Accordingly, the court adopts Hynix's proposed construction: "an erase operation" means "the removal of charge carriers from the floating gate of the memory cell."

V. *The* '111 patent

The '111 patent, issued on July 9, 1991, and subsequently reexamined on March 27, 2001, discloses a method and system for electronic design automation (EDA) that considers the interrelationships between the physical and electrical characteristics of an integrated circuit. The patent notes that "the present invention represents a significant advance in the field of design and fabrication of integrated circuits for operation at high frequencies * * *." ' 111 patent at 3:41-44. In particular, the patent states that it "provides a novel automated approach to the design of such circuits, using a knowledge based system to design circuits quickly based on user-supplied specifications." Id at 3:45-49. The patent also states that "[o]ther important aspects of the invention are its use of a unified data structure containing both the electrical and the physical characteristics of circuit elements in a single structure, to facilitate layout and other operations of the system, and its use of a circuit compaction technique to reduce the area occupied by the circuit without detracting from its electrical performance." Id at 3:49-55.

Although Hynix contends that none of the following terms need to be construed except for "unified data structure," Hynix has proposed constructions should the court decide to construe any of the other terms. All terms at issue appear only in claim 17, which was issued during the reexamination. That claim reads in full:

17. For use in a system for *automatically fabricating integrated circuits for operation at high frequencies,* an electronic design automation method comprising the steps of:

[1] A method for storing and retrieving data relating to circuit modules, comprising the steps of:

[a] partitioning a circuit into macrocells;

[b] partitioning the macrocells into microcells;

[c] partitioning the microcells into smaller microcells and *primitive circuit elements;*

[d] storing for each macrocell, microcell and primitive circuit element, data in a *universal format,* said data together defining electrical characteristics and interconnections, and physical characteristics and locations of the circuit modules, to form a complete *hierarchical definition* of the entire circuit, whereby circuit layout is facilitated because the electrical and physical characteristics are stored together in a *unified data structure;*

and

[2] A method for generating said circuit layout of a circuit module comprising the steps of:

[a] inputting at least one design parameter;

[b] defining at least one *constraint derived from said at least one design parameter* wherein compliance with said at least one constraint by said circuit layout prevents one or more undesirable effects on the electrical performance of said circuit modules;

[c] *considering at least one layout option;*

[d] determining whether said at least one layout option complies with said at least one constraint;

[e] if said layout option complies with at least one said constraint, performing said layout option.

Id at claim 17 (emphasis added on disputed terms) (bracketed numbers and letters added).

1. "automatically fabricating integrated circuits"

Hynix contends this term, if construed, should be defined as "making integrated circuits with machines that reduce the involvement of expert designers." Joint Cl Const, App 1 at 1. Toshiba instead contends that "automatically fabricating integrated circuits" means "[a] process that manufactures integrated circuits, without intervention by a human operator." Id. Both parties appear to assume that this term relates directly to the *design,* rather than the *fabrication* (i e, making), of integrated circuits.

Putting aside whether "automatically fabricating integrated circuits" should be construed because it only appears in the preamble of claim 17, Hynix Br at 21-22, both parties have misconceived this term. The "system for automatically fabricating integrated circuits" is a machine that fabricates the actual, physical integrated circuits. This conclusion follows from language in the preamble itself: "*an electronic design automation method*" produces a circuit design "*[f]or use* in a *system for automatically fabricating integrated circuits* for operation at high frequencies." Indeed, the specification teaches that the "electronic design automation method" of this patent creates as its end product "a coded tape, * * * which may be used to generate fabrication masks in a commercially available integrated circuit fabrication system." '111 patent at 5:17-20. See also id at abstract ("The method of the invention permits a relatively unskilled user to specify a circuit by performance parameters only, and to obtain as an end product a coded output that will drive a conventional mask fabrication system used to produce the circuit."). Because the present dispute centers on the integrated circuit *design* methodology taught by the patent, and because "system for automatically fabricating integrated circuits" relates to the *fabrication,* not the design of such circuits, the meaning of this term is irrelevant to the present dispute. Accordingly, the court presently declines to construe this term. If a dispute later arises between the parties regarding the fabrication process encompassed by the present invention, the court can revisit construction of this term at that time.

2. "integrated circuits for operation at high frequencies"

Hynix proposes this term, if construed, should be defined as "integrated circuits that function at frequencies where the physical and electrical characteristics of the circuit are closely interrelated." Joint Cl Const, App 1 at 4. Toshiba instead contends that "integrated circuits for operation at high frequencies" are limited to

"[m]icrowave and millimeter wave circuits, not including digital logic circuits." Id.

Toshiba's construction is problematic because it impermissibly limits the present invention to certain technologies. The patent states that "as a practical matter * * * it makes sense to apply the invention only to technologies and devices that operate at high enough frequencies to justify storing the component descriptions in a unified way * * *." '111 patent at 9:27-32. But the patent also explicitly recognizes that technologies other than microwave or millimeter wave circuit technologies could be used:

The circuit components are defined in the unified data structure in a manner that is not dependent on the technology involved. Therefore, the data structure, and indeed the [Microwave Monolithic Integrated Circuit] MUSIC approach to design, are equally applicable to other technologies.

Id at 9:23-27. Because Toshiba's construction conflicts with the specification and Hynix contends this term need not be construed, the court declines to construe the term.

3. "primitive circuit elements"

Hynix proposes this term, if construed, means "elements of a circuit at the lower levels of a hierarchical definition of the circuit, examples of which include a resistor, a capacitor, and inductor and a transistor." Joint Cl Const, App 1 at 8. Toshiba contends the term means "[m]icrowave or millimeter wave circuit topologies." Id.

As with the previous term, Toshiba's construction impermissibly limits the present invention to microwave or millimeter wave circuit technologies. See *supra* section V(2). Because Hynix does not believe this term needs construction, the court declines to construe the term.

4. "universal format"

Hynix contends that this term, if construed, should be defined as "an arrangement of data constituting all or many characteristics of a circuit." Joint Cl Const, App 1 at 10. Toshiba instead proposes a construction of "[p]ublicly available, vendor-independent, nonproprietary, arrangement of data for input or output." Id.

Toshiba does not cite intrinsic evidence in support of its excessively-detailed construction; rather, a dictionary definition-that "universal" means "used or understood by all"-is said to compel its proposal. Doc # 87 at 24. Yet the wide gap between this generic definition and Toshiba's detailed construction is left unexplained. Accordingly, the court follows Hynix's recommendation and declines to construe the term.

5. "hierarchical definition"

If this term is construed, Hynix proposes it should mean "specification of the design of a circuit through circuit elements of different levels of size or complexity, such as macrocells, microcells and primitive circuit elements." Joint Cl Const, App 1 at 12. Toshiba instead proposes a much more lengthy definition: "Partitioning a circuit into macrocells, partitioning the macrocells into microcells, partitioning the microcells into smaller microcells and primitive circuit elements, and storing for each macrocell, microcell and primitive circuit element, data in a unified format defining electrical characteristics and interconnections, and physical characteristics and locations of the circuit modules." Id.

Toshiba's long-winded construction is completely unnecessary because it almost verbatim incorporates

limitations that appear in the claim itself. See ' 111 patent at claim 17 ("a method * * * comprising steps of: partitioning a circuit into macrocells; partitioning the macrocells into microcells, partitioning the microcells into smaller microcells and primitive elements; storing for each macrocell, microcell and circuit element, data in a universal format, * * * defining electrical characteristics and interconnections, and physical characteristics and locations of the circuit modules"). Toshiba's construction provides no useful guidance as to the term's meaning and would simply confuse a jury.

Because Toshiba's construction is problematic and Hynix prefers not to construe this term, the court does not construe the term.

6. "unified data structure"

Hynix contends this term means, "a software system that enables access to electrical and physical characteristics of elements in a circuit design." Joint Cl Const, App 1 at 14. Toshiba again proposes a much more involved definition: "A file structure in which both physical and electrical characteristics of every circuit element are stored at any level of complexity together in the [sic] rationally consistent manner to facilitate circuit layout for use in a circuit compaction procedure." Id.

In its reply brief, Hynix attacks Toshiba's construction only on the basis that it impermissibly imports the limitation "for use in a circuit compaction procedure" from a dependent claim and thereby violates the doctrine of claim differentiation. See Doc # 92 (Hynix Reply Br) at 14. In its submission to the court in support of its *Markman* presentation, Hynix reiterated this argument and also correctly noted the modifier "file" was not supported by the intrinsic evidence. Hynix *Markman* submission, Ex 17. In response to Hynix's reply brief, Toshiba noted in its *Markman* submission that it would be willing to drop the phrase "for use in a circuit compaction procedure" from its proposed construction. Toshiba *Markman* submission, Ex 50.

Toshiba correctly suggests that the parties' current proposed constructions are highly similar. Toshiba's construction in particular is based directly on language in the abstract and claim 17. But the simplicity and straightforwardness of Hynix's proposed construction recommends its adoption in contrast to the relatively and unnecessarily prolix Toshiba proposal. Accordingly, the court adopts Hynix's construction of "unified data structure."

7. "constraint derived from said at least one design parameter"

Hynix proposes this term, if construed, means "limitation on a property of the circuit design." Joint Cl Const, App 1 at 17. Toshiba again proposes a lengthy definition: "A rule received or obtained from at least one design parameter that captures the designer's abilities and intuition wherein compliance with the rule avoids adverse effects on the electrical characteristics of the circuit and compacts the circuit to as small an area as possible while complying with the rule." *Id.*

Toshiba again provides a convoluted construction, defining a 9-word term with a construction that is 49 words long. And Toshiba's construction relies on phrases such as "designer's abilities and intuition" that seem more vague than the term itself. Moreover, the meaning of the term is clear enough from the claim and the specification: a constraint is, as Hynix states, a limitation on a property of circuit design. See '111 patent at FIGS 4 and 6; id at at 7:10-8:46. See also id at 8:12-14 ("The compaction procedure first sets up a set of simultaneous equations which describe the constraints of the layout problem."). Briefly, a user inputs a design parameter, from which a constraint is derived, and the program iterates until the proposed design

can no longer meet that constraint. See id at 7:10-8:46.

Because Toshiba's construction is unnecessary and Hynix does not seek construction of this relatively straightforward term, the court declines to construe the term.

8. "considering at least one layout option"

Hynix contends that this term, if construed, means "generating an approximation of the physical information of a circuit design." Joint Cl Const, App 1 at 20. Toshiba instead proposes the term means, "Simulate and optimize the performance of the physical design including the effects of the layout of distributed elements." Id.

Again, Toshiba has proposed an ambiguous and unnecessary construction. First, it is not clear what the phrase "distributed elements" means; indeed, this term does not even appear anywhere in the patent. Hence, Toshiba's construction would replace the present term with a more ambiguous one. Second, the meaning of "considering at least one layout option" would be clear to one having ordinary skill in the art in light of the specification, especially when compared to Toshiba's proposal. Accordingly, the court declines to construe the present term.

VI

In sum, the court has construed many of the disputed terms of the '311, ' 519, '190 and '111 patents according to the intrinsic record. The court declined to construe some terms because their meaning already was clear or was no longer ambiguous after the court had construed other related terms.

IT IS SO ORDERED.

N.D.Cal.,2006.
Hynix Semiconductor Inc. v. Toshiba Corp.

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