United States District Court, S.D. California.

QUALCOMM INCORPORATED, Plaintiff. v. BROADCOM CORPORATION, Defendants. Broadcom Corporation, Counter-Claimant. v. Qualcomm Incorporated, Counter-Defendant.

Civil No. 05CV1958-B(BLM)

June 20, 2006.

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CLAIM CONSTRUCTION ORDER FOR UNITED STATES PATENT NUMBER 5,452,104

RUDI M. BREWSTER, District Judge.

Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370(1996), on February 7-9, 2006, and March 14-16, 2006, the Court conducted a Markman hearing concerning the above-titled patent infringement action regarding construction of the disputed claim terms for U.S. Patent Number 5,452,104 ("the '104 patent"). Plaintiff Qualcomm, Inc. was represented by the law firm of Day Casebeer Madrid & Batchelder LLP, and Defendant Broadcom Corp. was represented by the law firm of Wilmer Cutler Pickering Hale and Dorr LLP.

At the Markman hearing, the Court, with the assistance of the parties, analyzed the claim terms in order to prepare jury instructions interpreting the pertinent claims at issue in the '104 patent. Additionally, the Court prepared a case glossary for terms found in the claims and specification for the '104 patent considered to be technical in nature which a jury of laypersons might not understand clearly without a specific definition.

After careful consideration of the parties' arguments and the applicable statutes and case law, the Court **HEREBY CONSTRUES** the claims in dispute for the '104 patent and **ISSUES** the relevant jury instructions as written in Exhibit A, attached hereto. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED.

EXHIBIT A FN1

FN1. All terms appearing in bold face type and underlined have been construed by the court and appear with their definitions in the glossary in Exhibit B. The definition for each construed term appears in italics after its first use in the patent.

VERBATIM CLAIM	COURT'S CONSTRUCTION
LANGUAGE	
Claim 3	Claim 3
3. In an adaptive block size	3. In an <i>adaptive block size compression system</i> [an apparatus capable
compression system wherein a	of use in compressing data organized in different block sizes] wherein a
block of pixel data is transformed	block of pixel data [a set of values specifying the brightness and/or
to AC and DC discrete cosine	color of pixels in a rectangular array of pixels. A pixel is a contraction
transform (DCT) coefficient data	of "picture element," the smallest addressable element in an electronic
for a block and constituent sub-	display .] is transformed to AC and DC discrete cosine transform
blocks of pixel data, and wherein	(DCT) [DCT is a mathematical transform that converts data into a set
the AC and DC DCT coefficient	of coefficients that are derived from equations (1), (2) and (3) set forth
values of a composite block of	in the '104 patent in col. 4, line 60 to col. 5, line 4. DC DCT coefficient
selected ones of said block and	is the weighted average of the data input into the DCT. The AC DCT
constituent sub-blocks of pixel data	coefficient is any DCT coefficient other than a DC DCT coefficient.]
are provided for transmission, an	coefficient data for a block and <i>constituent sub-blocks</i> [constituent
apparatus for compressing said DC	sub-block is a part of a block resulting from a partitioning of the block
DCT coefficient values comprising:	into multiple contiguous, adjacent, nonoverlapping parts] of pixel data
	[values specifying the brightness and/or color of one or more pixels],
	and wherein the AC and DC DCT coefficient values of a composite
	block of selected ones of said block and constituent sub-blocks of <i>pixel</i>
	<i>data</i> are provided for transmission, an apparatus for compressing said
	DC DCT coefficient values comprising [including but not limited to]:
discrete quadtree means for	discrete quadtree means [This is a means-plus-function limitation as
receiving at least one block of	discussed below] for receiving at least one block of data representing
data representing said block of	said <i>block of pixel data</i> , performing a <i>plurality</i> [<i>two or more</i>] of <i>DCT</i>
pixel data, performing a plurality	operations to provide AC and DC DQT coefficient [A DC DQT

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of DCT operations to provide AC and DC DQT coefficient values, with a first DCT operation performed on said at least one block of data to provide first sub-blocks of AC and DC DQT coefficient values, performing at least one additional DCT operation wherein each of said at least one additional DCT operation is performed on resultant DC DQT coefficient data of a preceding DCT operation, and selecting ones of AC and DC DQT coefficient values to provide a DQT composite block of AC and DC coefficient values; and

coefficient is the coefficient output from a DCT operation in the DQT that is a weighted average of the data input into that DCT operation. An **AC DQT coefficient** is any coefficient output from a DCT operation in the DQT other than the DC DQT coefficient.] values, with a first **DCT** operation performed on said at least one block of data to provide first sub-blocks of **AC and DC DQT coefficient** values, performing at least one additional **DCT** operation wherein each of said at least one additional **DCT** operation is performed on resultant **DC DQT coefficient** data of a preceding **DCT** operation, and selecting ones of **AC and DC DQT coefficient** values to provide a **DQT composite block of AC and DC coefficient** values [a series of AC and DC coefficient values determined from successive stages of the DQT]; and

" Discrete quadtree means for receiving at least one block of data representing said block of pixel data, performing a plurality of DCT operations to provide AC and DC DQT coefficient values, with a first DCT operation performed on said at least one block of data to provide first sub-blocks of AC and DC DQT coefficient values, performing at least one additional DCT operation wherein each of said at least one additional DCT operation is performed on resultant DC DQT coefficient data of a preceding DCT operation, and selecting ones of AC and DC DQT coefficient values to provide a DOT composite block of AC and DC coefficient values " is a means-plus function limitation. [This means-plus-function limitation has four functions. The first function of this limitation is: (1) receiving at least one block of data representing said block of pixel data. The corresponding structure that performs the first function is an input into the DQT subsystem or an input into the DCT element of a DQT subsystem.

The second and third functions of this limitation are: (2) performing a plurality of **DCT** operations to provide AC and DC **DQT** [discrete quadtree transform: a sequence of two or more two-dimensional discrete cosine transforms that operate on a quadtree structure of a block of pixel data and/or coefficient data derived from a block of pixel data. A **quadtree** is a division of a block into one or more levels of four sub-blocks ("nodes"), such that each could be, but is not required to be, further sub-divided into four further nodes] coefficient values, with a first **DCT** operation performed on said at least one block of data to provide first sub-blocks of **AC and DC DQT coefficient** values and (3) performing at least one additional **DCT** operation wherein each of said

	at least one additional DCT operation is performed on resultant DC
	DQT coefficient data of a preceding DCT operation.
	The corresponding structure for the second and third functions is one or
	more of the DCT elements of Figure 6 (DCT elements 70, 74, 78, and/or 84) not limited to an aution on 222 sized sub blocks. Col. 4, 28, 52
	(DCT Ferminica to operation on 2x2 sized sub-blocks; Col. 4:58-52
	(DCT Formula); Col. 9:67-10:1 ("DCT elements 10a-10a may be
	constructed in integrated circuit form as is well known in the art"); Col
	17:10-58 and Figure 1 and Figure 6 (the same block of pixel data is
	received in the DQI subsystem); Col. 8:40-38 ("various block sizes
	may be used, "including N x N, N x M, and odd integer-sized blocks much as $0 = 0$. Col. 0.49, 52 (N = N mixed data is isomet to the DOT
	such as 9×9 ; Col. 9:40-32 (N \times N pixel data is input to the DQ1 submatem and N = 16 for purposes of illustration); Figure 1 (16 \times 16
	subsystem and $N = 10$ for purposes of illustration); Figure 1 (10 x 10 DIVEL DLOCK EDOM EDAME DLIEFED, and arrows "TO DOT
	FIAEL DLOCK FROM FRAME DUFFER, and arrow TO DQT SUPSYSTEM!, and Eigung 6 (16 x 16 DIVEL DLOCK)
	SUBSISIEM), and Figure 0 (10 x 10 FIXEL BLOCK).
	The fourth function of this limitation is: (4) selecting ones of AC and
	DC DQT coefficient values to provide a DQT composite block of AC
	and DC coefficient values.
	The corresponding structure for the fourth function is a multiplexer.]
encoding means for receiving said DQT composite block, selecting values from said DQT composite block and encoding said selected values of said DQT composite block to provide a signal indicative of compressed DC DCT coefficient values.	 encoding means for receiving said DQT composite block, selecting values from said DQT composite block and encoding said selected values of said DQT composite block to provide a signal indicative of compressed DC DCT coefficient values [This is a means plus function limitation. This means-plus-function limitation has three functions. The first function of this limitation is receiving said DQT composite block. The corresponding structure for the first function is an input into a selector or a multiplexer. The second function is selecting values from said DQT composite block. The corresponding structure for the second function is a selector or a
	multiplexer.
	The third function is encoding said selected values of said DQT composite block to provide a signal indicative of compressed DC DCT coefficient values.
	The corresponding structure for the third function is a code lookup table or a code length lookup table.].
Claim 4	Claim 4
4. The apparatus of claim 3	The apparatus of claim 3 wherein said discrete quadtree means comprises:
wherein said discrete quadtree	
means comprises:	
at least one DCT means for receiving said at least one block of data and performing	at least one DCT means for receiving said at least one block of data and performing a series of DCT operations to provide AC and DC DQT coefficient values with a first DCT operation performed on said at least
a series of DCT operations to provide AC and DC DQT coefficient values with a first	one block of data and with additional DCT operations performed on sub- blocks of selected DC DQT coefficient values [This is a means plus function limitation. This means-plus-function limitation has two functions.

DCT operation performed on said at least one block of data and with additional DCT operations performed on subblocks of selected DC DQT coefficient values; and

The first function of this limitation is receiving said at least one block of data.

The corresponding structure for the first function is an input into the **DQT** subsystem or an input into the **DCT** element of a **DQT** subsystem.

The second function of this limitation is performing a series of DCT operations to provide AC and DC DQT coefficient values with a first DCT operation performed on said at least one block of data and with additional DCT operations performed on sub-blocks of selected DC DOT coefficient values.

	The corresponding structure for the second function is one or more of the DCT elements of Figure 6 (DCT elements 70, 74, 78, and/or 84) not limited to operation on 2 x 2 sized sub-blocks; Col. 4:38-52 (DCT Formula); Col. 9:67-10:1 ("DCT elements 10a-10d may be constructed in integrated circuit form as is well known in the art"); Col 17:16-58 and Figure 1 and Figure 6 (the same block of pixel data is received in the DOT subsystem; Col. 8:46-58 ("various block sizes may be used," including N x N, N x M, and odd integer-sized blocks such as 9 x 9); Col. 9:48-52 (N x N pixel data is input to the DQT subsystem and N=16 for purposes of illustration); Figure 1 (16 x 16 PIXEL BLOCK FROM FRAME BUFFER, and arrow "TO DOT SUBSYSTEM"): and Figure 6 (16 x 16 PIXEL BLOCK).]: and
selector means for receiving said AC and DC DQT coefficient values selecting ones of said AC and DC DQT, coefficient values to provide said sub-blocks of selected DC DQT coefficient values in accordance with a predetermined selection format.	selector means for receiving said AC and DC DQT coefficient values selecting ones of said AC and DC DQT, coefficient values to provide said sub-blocks of selected DC DOT coefficient values in accordance with a predetermined selection format [This is a means plus function limitation. This means-plus function limitation has two functions. The first function of this limitation is receiving said AC and DC DQT coefficient values.

The corresponding structure of the first function is an input into a selector or a multiplexer.

The second function of this limitation is selecting ones of said AC and DC DQT coefficient values to provide said subblocks of selected DC DQT

coefficient values in accordance with a predetermined selection format.

The corresponding structure of the second function is a selector or a multiplexer.].

пширислег.ј.	
Claim 5	Claim 5
5. The apparatus of claim 4 wherein said at least one	5. The apparatus of claim 4 wherein said at least one
DCT means comprises a plurality of single DCT	DCT means comprises a plurality of single DCT
means wherein each of said single DCT means is for	means wherein each of said single DCT means is for
performing a corresponding one of said series of	performing a corresponding one of said series of DCT
DCT operations.	operations.
Claim 7	Claim 7
7. The apparatus of claim 3 wherein said at least one	7. The apparatus of claim 3 wherein said at least one
block of data comprises pixel data.	block of data <i>comprises pixel data</i> .
Claim 13	Claim 13
13. In an adaptive block size compression system	13. In an <i>adaptive block size compression system</i>
wherein a block of pixel data is transformed to AC	wherein a block of pixel data is transformed to AC and
and DC discrete cosine transform (DCT) coefficient	DC discrete cosine transform (DCT) coefficient data
data for a block and at least one constituent level of	for a block and at least one constituent level of sub-
sub-blocks of pixel data, and wherein the AC and	blocks of pixel data, and wherein the AC and DC DCT
DC DCT coefficient values of a composite block of	<i>coefficient</i> values of a composite block of selected
selected ones of said block and constituent sub-	ones of said block and <i>constituent sub-blocks</i> of pixel
blocks of pixel data are provided for transmission, a	data are provided for transmission, a method for
method for compressing said DC DCT coefficient	compressing said <i>DC DCT coefficient</i> values
values comprising:	comprising:
receiving at least one block of data;	receiving at least one block of data;
performing a series of discrete cosine transformation	performing a series of discrete cosine transformation (
(DCT) operations to provide AC and DC DQT	DCT) operations to provide AC and DC DQT
coefficient values with a first DCT operation	coefficient values with a first DCT operation
performed on said at least one block of data to	performed on said at least one block of data to provide
provide first sub-blocks of AC and DC DOT	first sub-blocks of AC and DC DQT coefficient values
coefficient values and at least one additional DCT	and at least one additional DCT operations is
operations is performed on sub-blocks of selected	performed on sub-blocks of selected <i>DC DQT</i>
DC DQT coefficient values resultant from a	coefficient values resultant from a preceding DCT
preceding DCT operation of said series of DCT	operation of said series of <i>DCT</i> operations; and
operations; and	
selecting ones of AC and DC DQT coefficient	selecting ones of AC and DC DQT coefficient values
values resultant from said first DCT operation and	resultant from said first DCT operation and said at least
said at least one additional DCT operation to provide	one additional <i>DCT</i> operation to provide a <i>DQT</i>
a DQT composite block of AC and DC DQT	composite block of AC and DC DQT coefficient
coefficient values.	values.
Claim 59 Claim 59	Claim 59
59. In an image decoder wherein an image block 5	9. In an image decoder wherein an image block of pixel
of pixel data is processed by performing a discrete d	ata is processed by performing a discrete cosine
cosine transform (DCT) operation on said block of the	ransform (DCT) operation on said block of pixel data
pixel data and on at least one predetermined level a	nd on at least one predetermined level of constituent
of constituent sub-blocks of pixel data thereof, and such	ub-blocks of pixel data thereof, and providing
providing corresponding block and sub-blocks of c	orresponding block and sub-blocks of AC and DC DCT

AC and DC DCT coefficient value	s and wherein	coefficient values and wherein said DC DCT coefficient
said DC DCT coefficient values is	further	values is further processed by performing <i>a series of at</i>
processed by performing a series of	f at least one	least one additional DCT operation [one or more DCT
additional DCT operation on said s	ub-blocks of	operations] on said sub-blocks of DC DCT coefficient
DC DCT coefficient values, a subs	ystem for	values, a subsystem for decoding said processed DC
decoding said processed DC DCT	coefficient	DCT coefficient values comprising:
values comprising:		
decoder means having an input for	receiving a	decoder means [an element capable of translating
signal indicative of said processed	DC DCT	coded data to unencoded data] having an input for
coefficient values and having an ou	tput; and	receiving a signal indicative of said processed <i>DC DCT</i> <i>coefficient</i> values and having an output; and
inverse discrete quadtree means have	ving an input	inverse discrete quadtree means [an element capable of
coupled to said decoder means outp	out, wherein said	determining the inverse of a discrete quadtree transform,
inverse discrete quadtree means con	mprises:	by using a sequence of two or more inverse discrete
		cosine transform operations to convert a block of DQT
		coefficients into a block of pixel data] having an input
		coupled to said <i>decoder means</i> output, wherein said
		inverse discrete quadtree means comprises:
plurality of separator means with a	first separator	<i>plurality</i> of <i>separator means</i> [an element capable of
means having an input for receiving	g said signal	selecting and extracting coefficients from a stage of an
indicative of said processed DC DC	CT coefficient	inverse DQT computation] with a first separator means
values and additional separator mea	ans having an	having an input for receiving said signal indicative of
input and an output;		said processed DC DCT coefficient values and additional
		separator means having an input and an output;
at least one inverse discrete means	disposed	at least one <i>inverse discrete means</i> [an element capable
between said plurality of separator means having		of performing an inverse discrete cosine transform]
an input coupled to a corresponding separator		disposed between said <i>plurality</i> of <i>separator means</i>
means output.		having an input coupled to a corresponding <i>separator</i>
		<i>means</i> output.
Claim 60	Claim 60	
60. The apparatus of claim 59	60. The appara	tus of claim 59 wherein said <i>separator means</i> further
wherein said separator means	having a secon	d output and wherein said <i>discrete quadtree means</i>
turther having a second output and	further <i>comprus</i>	ses:
wherein said discrete quadtree		
means further comprises:		
at least one multiplexer means	at least one <i>mu</i>	altiplexer means [an element capable of selecting one of
having an input for receiving a	a number of in	put signals and routing that input signal's information to
timing signal, a second input	the multiplexer	's output] having an input for receiving a timing signal [
coupled to a corresponding	a signal capab	le of conveying timing information], a second input
inverse cosine transform means	coupled to a co	orresponding <i>inverse cosine transform means</i> [an
output and a third input coupled		A AL NARIARMAINA AN INNARRA ALGORATA AAGINA TRANSTARMA
to a company ding correct	element capabl	ind input coupled to a company ding second constraints
to a corresponding second	output and a th	ird input coupled to a corresponding second <i>separator</i>

EXHIBIT B

UNITED STATES PATENT NUMBER 5,452,104-GLOSSARY OF TERMS

TERM	DEFINITION
AC and DC discrete cosine transform (DCT) DCT is a mathematical transform that converts data into a
``	set of coefficients that are derived from equations (1), (2)
	and (3) set forth in the '104 patent in col. 4, line 60 to col. 5.
	line 4. DC DCT coefficient is the weighted average of the
	data input into the DCT. The AC DCT coefficient is any
	DCT coefficient other than a DC DCT coefficient.
AC DCT coefficient	any DCT coefficient other than a DC DCT coefficient
AC and DC DOT coefficient	A DC DOT coefficient is the coefficient output from a DCT
	operation in the DOT that is a weighted average of the data
	input into that DCT operation. An AC DOT coefficient is
	any coefficient output from a DCT operation in the DOT
	other than the DC DOT coefficient.
AC DOT coefficient	any coefficient output from a DCT operation in the DOT
	other than the DC DOT coefficient
adaptive block size compression system	an apparatus capable of use in compressing data organized
auprive sheet size compression system	in different block sizes
a series of at least one additional DCT	one or more DCT operations
operation	one of more Dell operations
block of nivel data	a set of values specifying the brightness and/or color of
block of place data	nixels in a rectangular array of nixels [A nixel is a
	contraction of "nicture element" the smallest addressable
	element in an electronic display]
20mmileog	See definition of "comprising "
	See definition of comprising.
constituent sub-blocks	constituent sub-block is a part of a block resulting from a
	partitioning of the block into multiple contiguous, adjacent,
	non-overlapping parts
DC DCT coefficient	the weighted average of the data input into the DCT.
DC DQT coefficient	the coefficient output from a DCT operation in the DQT
	that is a weighted average of the data input into that DCT
	operation
DCT	discrete cosine transform. DCT is a mathematical transform
	that converts data into a set of coefficients that are derived
	from equations (1), (2) and (3) set forth in the '104 patent in
	col. 4, line 60 to col. 5, line 4.
DCT means for receiving said at least one	This is a means plus function limitation. This means-
block of data and performing a series of	plus-function limitation has two functions.
DCT operations to provide AC and DC	
DQT coefficient values with a first DCT	
operation performed on said at least one	
block of data and with additional DCT	
operations performed on sub-blocks of	
selected DC DQT coefficient values	
	The first function of this limitation is receiving said at least
	one block of data. The corresponding structure for the first

function is an input into the DQT subsystem or an input into the DCT element of a DQT subsystem.

The second function of this limitation is performing a series of <i>DCT</i> operations to provide <i>AC</i> and <i>DC DQT</i> coefficient values with a first <i>DCT</i> operation performed on said at least one block of data and with additional <i>DCT</i> operations performed on sub-blocks of selected <i>DC DQT</i> coefficient values.	
	or more of the DCT elements of Figure 6 (DCT elements 70, 74, 78, and/or 84) not limited to operation on 2 x 2 sized sub-blocks; col. 4:38-52 (DCT Formula); col. 9:67-10:1 ("DCT elements 10a-10d may be constructed in integrated circuit form as is well known in the art"); col. 17:16-58 and Figure 1 and Figure 6 (the same block of pixel data is received in the DOT subsystem; col. 8:46-58 ("various
	block sizes may be used," including N x N, N x M, and odd integer-sized blocks such as 9 x 9); col. 9:48-52 (N x N pixel data is input to the DQT subsystem and N=16 for purposes of illustration); Figure 1 (16 x 16 PIXEL BLOCK FROM FRAME BUFFER, and arrow "TO DQT SUBSYSTEM"); and Figure 6 (16 x 16 PIXEL BLOCK).]
DCT means	See definition of "DCT means for receiving said at least one block of data and performing a series of DCT operations to provide AC and DC DQT coefficient values with a first DCT operation performed on said at least one block of data and with additional DCT operations performed on sub-blocks of selected DC DOT coefficient values."
decoder means	an element capable of translating coded data to unencoded data
discrete quadtree means for receiving at least one block of data representing said block of pixel data, performing a plurality of DCT operations to provide AC and DC DQT coefficient values, with a first DCT operation performed on said at least one block of data to provide first sub-blocks of AC and DC DQT coefficient values, performing at least one additional DCT operation wherein each of said at least one additional DCT operation is performed on resultant DC DQT coefficient data of a preceding DCT operation and selecting	This is a means-plus-function limitation. This means-plus- function limitation has four functions. The first function of this limitation is: (1) receiving at least one block of data representing said <i>block of pixel data</i> .

ones of AC and DC DQT coefficient

values to provide a DQT composite block of AC and DC coefficient values

The corresponding structure that performs the first function is an input into the DQT subsystem or an input into the DCT element of a DQT subsystem.

The second and third functions of this limitation are: (2) performing a plurality of **DCT** operations to provide AC and DC DQT [discrete quadtree transform: a sequence of two or more two-dimensional discrete cosine transforms that operate on a quadtree structure of a block of pixel data and/or coefficient data derived from a block of pixel data. A *quadtree* is a division of a block into one or more levels of four sub-blocks ("nodes"), such that each could be, but is not required to be, further sub-divided into four further nodes] coefficient values, with a first **DCT** operation performed on said at least one block of data to provide first sub-blocks of *AC and DC DQT coefficient* values and (3) performing at least one additional **DCT** operation wherein each of said at least one additional **DCT** operation is performed on resultant **DC DQT coefficient** data of a preceding **DCT** operation.

The corresponding structure for the second and third functions is one or more of the DCT elements of Figure 6 (DCT elements 70, 74, 78, and/or 84) not limited to operation on 2 x 2 sized sub-blocks; Col. 4:38-52 (DCT Formula); Col. 9:67-10:1 ("DCT elements 10a-10d may be constructed in integrated circuit form as is well known in the art"); Col. 17:16-58 and Figure 1 and Figure 6 (the same block of pixel data is received in the DQT subsystem); Col. 8:46-58 ("various block sizes may be used," including N x N, N x M, and odd integer-sized blocks such as 9 x 9); Col. 9:48-52 (N aN pixel data is input to the DQT subsystem and N=16 for purposes of illustration); Figure 1 (16x16 PIXEL BLOCK FROM FRAME BUFFER, and arrow "TO DQT SUBSYSTEM"); and Figure 6 (16 x 16 PIXEL BLOCK).

The fourth function of this limitation is: (4) selecting onesof % AC and DC DQT coefficient values to provide a DQTcomposite block of AC and DC coefficient values.The corresponding structure for the fourth function is a
multiplexer.

	mulliplexer.
discrete quadtree means	See definition of "Discrete quadtree means for receiving
	at least one block of data representing said block of
	pixel data, performing a plurality of DCT operations to

	provide AC and DC DQT coefficient values, with a first DCT operation performed on said at least one block of
	data to provide first sub-blocks of AC and DC DQT
	coefficient values, performing at least one additional
	DUI operation wherein each of said at least one additional DCT operation is performed on resultant DC
	DOT coefficient data of a proceeding DOT operation and
	selecting ones of AC and DC DOT coefficient values to
	provide a DOT composite block of AC and DC
	coefficient values."
ООТ	(discrete quadtree transform): a sequence of two or more
	two-dimensional discrete cosine transforms that operate on
	a quadtree structure of a block of pixel data and/or
	coefficient data derived from a block of pixel data. A
	<i>quadtree</i> is a division of a block into one or more levels of
	four sub-blocks ("nodes"), such that each could be, but is
	not required to be, further sub-divided into four further
	nodes.
DQT composite block of AC and DC	a series of AC and DC coefficient values determined from
coefficient values	successive stages of the DQT
encoding means for receiving said DQT	This is a means plus function limitation. This means-
composite block, selecting values from	plus-function limitation has three functions.
said DQT composite block and encoding	
said selected values of said DQT	
composite block to provide a signal	
indicative of compressed DC DCT	
coefficient values	
	The first function of this limitation is receiving said DOT
	composite block. The corresponding structure for the first
	function is an input into a selector or a multiplexer.
	The second function is selecting values from said DQI
	composite block. The corresponding structure for the
	second function is a selector of a multiplexer.
	The third function is encoding said selected values of said
	DOT composite block to provide a signal indicative of
	compressed <i>DC DCT coefficient</i> values. The corresponding
	structure for the third function is a code lookup table or a
	code length lookup table.
inverse cosine transform means	an element capable of performing an inverse discrete cosine
	transform
inverse discrete means	an element capable of performing an inverse discrete cosine
	transform
inverse discrete quadtree means	an element capable of determining the inverse of a discrete
	quadtree transform, by using a sequence of two or more

	inverse discrete cosine transform operations to convert a
	block of DQT coefficients into a block of pixel data
multiplexer means	an element capable of selecting one of a number of input
	signals and routing that input signal's information to the
	multiplexer's output
pixel	a contraction of "picture element," the smallest addressable
	element in an electronic display
pixel data	values specifying the brightness and/or color of one or more
	pixels
plurality	two or more
quadtree	a division of a block into one or more levels of four sub-
	blocks ("nodes"), such that each could be, but is not
	required to be, further sub-divided into four further nodes
selector means for receiving said AC and	This is a means plus function limitation. This means-
DC DQT coefficient values selecting ones	plus-function limitation has two functions.
of said AC and DC DQT, coefficient	
values to provide said sub-blocks of	
selected DC DQT coefficient values in	
accordance with a predetermined selection	
format	
	The first function of this limitation is receiving said <i>AC</i> and <i>DC DOT coefficient</i> values.
	The corresponding structure or the first function is an input
	into a selector or a multiplexer.
	The second function of this limitation is selecting ones of
	said AC and DC DQT coefficient values to provide said
	sub-blocks of selected DC DQT coefficient values in
	accordance with a predetermined selection format.
	The corresponding structure of the second function is a
	selector or a multiplexer.
separator means	an element capable of selecting and extracting coefficients
	from a stage of an inverse DQT computation
timing signal	a signal capable of conveying timing information

S.D.Cal.,2006. Qualcomm Inc. v. Broadcom Corp.

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