United States District Court, S.D. California.

QUALCOMM INCORPORATED, Plaintiff. v. CONEXANT SYSTEMS, INC.

and

Skyworks Solutions, Inc, Defendants.

No. 02CV2002-B(JFS)

Dec. 2, 2004.

James R. Batchelder, Day Casebeer Madrid and Batchelder, Cupertino, CA, for Plaintiff.

James L. Quarles, III, Kyle M. Deyoung, Nina S. Tallon, Amy K. Wigmore, Gregory S. Discher, Leon B. Greenfield, Wilmer Cutler Pickering Hale and Dorr, Washington, DC, Donald R. Steinberg, Michael A. Diener, Merriann M. Panarella, William F. Lee, Wilmer Cutler Pickering Hale and Dorr, Boston, MA, Kerry A. Malloy, S. Calvin Walden, Hale and Dorr, New York, NY, Maria Kathleen Vento, Wilmer Cutler Pickering Hale and Dorr LLP, Palo Alto, CA, Robert S. Brewer, Jr., McKenna Long and Aldridge, San Diego, CA, for Defendants.

ORDER CONSTRUING CLAIMS FOR UNITED STATES PATENT NUMBER 5,872,481

RUDI M. BREWSTER, Senior District Judge.

Plaintiff, Qualcomm, Inc. has brought suit against Defendants, Conexant Systems, Inc. and Skyworks Solutions, Inc., for infringement of United States Patent number 5,872,481 (the "'481 Patent"). Pursuant to Markman v. Westview Instruments, 52 F.3d 967 (Fed.Cir.1995), the Court conducted a hearing on October 14 and November 9, 2004 to construe the disputed claim terms of the '481 Patent. FN1 At the hearing, Qualcomm was represented by the law firm of Day, Casebeer, Madrid & Batchelder, and Conexant and Skyworks were represented by the firm of Wilmer, Cutler, Pickering and Dorr.

FN1. The disputed claims of the '481 Patent are claims 1-8.

The Court, with the assistance of the parties, interpreted the pertinent terms for all claim terms at issue in the '481 Patent. Additionally, a "Glossar" was prepared for terms found in the '481 Patent, that were considered

to be technical in nature and which a jury of laypersons might not understand without a specific definition, As the case advances, the parties may request additional terms to be added to the glossary as may seem helpful to the jury.

After careful consideration of the parties' arguments and the applicable law, the Court **HEREBY CONSTRUES** all disputed claim terms in the '481 Patent, attached as Exhibit A. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED

EXHIBIT A-UNITED STATES PATENT NUMBER 5,872,481-CLAIM CHART

| VERBATIM CLAIM LANGUAGE | COURT'S CLAIM CONSTRUCTION |
|--|--|
| Claim 1 | Claim 1 |
| An amplifier circuit for providing an | An amplifier [a device capable of increasing the power of a |
| amplified signal n response to a radio | signal] circuit [a network of electronic components] for providing |
| frequency (RF) input signal having | an amplified signal [information that can be transmitted or |
| successive portions separated by | received within a circuit] in response to a radio frequency (RF) |
| signal boundaries, said amplifier | [frequency useful for radio communication] input signal [signal |
| circuit comprising: | input to an electronic component] having successive portions |
| | [discrete parts that follow each other in order] separated by signal |
| | boundaries [border or transition between the digital words or |
| | symbols in a signal], said amplifier circuit comprising: |
| a timing information input line | a timing information input line receiving timing information |
| receiving timing information | representative of the boundaries between the portions of the RF |
| representative of the boundaries | input signal [an electrical line that receives information that |
| between the portions of the RF input | represents the periods during which there are boundaries in the |
| signal; | RF input signal]; |
| a plurality of amplifier stages for | a plurality [two or more] of amplifier stages for amplifying said RF |
| amplifying said RF signal, each of | signal, each of said plurality of amplifier stages having an amplifier |
| said plurality of amplifier stages | stage [a set of one or more amplifiers within an amplifier circuit |
| having an amplifier stage input for | containing at least two such sets] input [part of a device capable |
| receiving said RF input signal and an | of receiving a signal] for receiving said RF input signal and an |
| amplifier stage output for providing | amplifier stage output for providing an amplified RF signal, each of |
| an amplified RF signal, each of said | said amplifier stages operative to amplify the RF input signal only |
| amplifier stages operative to amplify | while a direct current (DC) [an electric current, constant over |
| the RF input signal only while a | some time period] bias [a signal delivered to an amplifier for |
| direct current (DC) bias is applied to | establishing the amplifier's operating point] is applied to the |
| the respective amplifier stage input | respective amplifier stage input thereof [the bias is applied to the |
| thereof: | same input that receives the RF input signal]: |
| a control circuit, coupled to each | a control circuit [a circuit for providing control], coupled to |
| amplifier stage input of said plurality | [associated in such a way that power or signal information may |
| of amplifier stages and to the timing information input line, for selecting | be transferred from one to another] each amplifier stage input of said plurality of amplifier stages and to the timing information input |
| particular amplifier stages to be | line, for selecting particular amplifier stages [selecting more than |
| | one amplifier stage] to be activated and for providing a DC bias to |
| to the amplifier input stages of each | the amplifier input stages of each of the selected amplifier stages |
| to the amplitude input stages of each | and amplitude input stages of each of the selected amplitude stages |

| of the selected amplifier stages, said control circuit operative to vary the selection of particular amplifier stage only during a boundary between portions of the RF input signal; and means, coupled to each of said amplifier stage inputs, for isolating said DC bias from the amplifier input stages of other ones of said plurality of amplifier stages. | vary the selection of particular amplifier stages only during a ges boundary between portions of the RF input signal; and means, coupled to each of said amplifier stage inputs, for isolating |
|--|--|
| | This is a means plus function claim. |
| | The function of the means is: isolating said DC bias from the amplifier input stages of other ones of said plurality of amplifier stages [electrically separating the DC bias provided to the selected stages from the inputs of non-selected stages] |
| | The structure(s) identified to perform this function is: Fig. 11, capacitors 1112, 1114, 1116, and 1118; 2:60-62; 9:60-10:5 |
| Claim 2 | Claim 2 |
| | her The amplifier circuit of claim 1 further comprising an input |
| | g annetwork [group of electronic components associated with the |
| | a input of a device], having an input coupled to [associated in such |
| plurality of outputs, each output | a way that power or signal information may be transferred from |
| coupled to one of said amplifier sta | • • • |
| | dingoutput coupled to one of said amplifier stage inputs, said input |
| said input signal to each of said | network for providing said input signal to each of said plurality of |
| plurality of amplifier stages; and | amplifier stages; and |
| | |
| an output network, coupled to each | |
| said amplifier stage outputs, for | with the output of a device], coupled to each of said amplifier |
| providing said amplified signal from | |
| - | y of least one of said plurality of amplifier stages at an output node [a |
| amplifier stages at an output node. | node (location where one or more signals is input and one or |
| | more signals is output) whose output is the output of the |
| | referenced circuit]. |
| Claim 3 | Claim 3 |
| 1 | The amplifier circuit of claim 2 wherein said means for isolating |
| | omprises a plurality of capacitors [devices capable of storing energy |
| | n the form of an electric field or charge. A capacitor is capable of |
| | locking the flow of direct current and passing or partially conducted |
| | he flow of a time-varying current], each capacitor having an input |
| | ignal, and an output coupled to a respective one of said amplifier stage |
| | nputs. |
| Claim 4 | Claim 4 |
| The amplituer circuit of [The ampli | fier circuit of claim 3 wherein at least on of said plurality of amplifier |

| amplifier stages is a field-effect transistor | from the source node to the drain node is controlled by an electric field caused by a voltage applied to the gate node] device. |
|---|---|
| device. | a voluge applied to the gate houes at the |
| Claim 5 | Claim 5 |
| claim 3 wherein at least one of said plurality of amplifier stages is a | The amplifier circuit of claim 3 wherein at least one of said plurality of amplifier stages is a bipolar junction transistor [a transistor having at least three nodes (called the base, collector, and emitter) in which the amount of current flowing from the collector node to the emitter node is controlled by the voltage across the junction between the base node and the emitter node] device. |
| Claim 6 | Claim 6 |
| amplified signal in response to a radio frequency (RF) input signal having successive portions separated by boundaries in an amplific circuit comprising a plurality of amplifier stages each operative to amplify a signal only while simultaneously receiving a direct current (DC) bias signal, said method comprising the steps of: | |
| - | receiving timing information representative of the boundaries between the e portions of the RF input signal [information that represents the periods n during which there are boundaries in the RF input signal]; |
| applying said input signa to each of said plurality o amplifier stages; | |
| selecting an amplifier stage for use in amplifyin the signal; | |
| applying a DC bias signa to the selected amplifier stage, with said DC bias signal being initiated during a boundary between portions of the | 1 applying a DC bias signal to the selected amplifier stage, with said DC bias signal being initiated during a boundary between portions of the RF input signal [border or transition between the digital words or symbols]; |

| signal from all but said selected one of said | of other all ampl | g said DC bias signal from all but said selected one of said plurality amplifier stages [the applied DC bias is separated electrically from lifier stages except the selected one]; |
|--|----------------------|---|
| plurality of other amplifier stages; | | |
| | amplifie | ng said input signal in said selected amplifier stage to generate said d signal; and |
| providing said amplified signal at an output node. | providin | g said amplified signal at an output node. |
| Claim 7 | | Claim 7 |
| The amplifier circuit of cla wherein said portions of th RF signals are words. | | The amplifier circuit of claim 1 wherein said portions of the input RF signals are words [a set number of data symbols or characters transmitted together as a group]. |
| Claim 8 | | Claim 8 |
| The method of claim 6 whe | erein | The method of claim 6 wherein said portions of the input RF signals |

EXHIBIT B-GLOSSARY RE: UNITED STATES PATENT NUMBER 5.872.481

| Term Definition | |
|-------------------------------------|--|
| Amplifier | A device capable of increasing the power of a signal |
| Amplifier Stage(s) | A set of one or more amplifiers within an amplifier circuit |
| | containing at least two such sets |
| Applied to the Respective Amplifier | The bias is applied to the same input that receives the RF input |
| Stage Input Thereof | signal |
| Bias | A signal delivered to an amplifier for establishing the amplifier's |
| | operating point |
| Bipolar Junction Transistor | A transistor having at least three nodes (called the base, collector, |
| | and emitter) in which the amount of current flowing from the |
| | collector node to the emitter node is controlled by the voltage across |
| | the junction between the base node and the emitter node |
| Boundaries | Border or transition between the digital words or symbols |
| Boundary Between Portions of the RF | Border or transition between the digital words or symbols |
| Input Signal | |
| Capacitors | Devices capable of storing energy in the form of an electric field or |
| | charge. A capacitor is capable of blocking the flow of direct current |
| | and passing or partially conducted the flow of a time-varying |
| | current |
| Control Circuit | A circuit for providing control |
| Coupled to | Associated in such a way that power or signal information may be |
| | transferred from one to another |
| Circuit | A network of electronic components |

| Field-effect TransistorA transistor having at least three nodes (called the gate source, a drain) in which the amount of current flowing from the source n to the drain node is controlled by an electric field caused by a voltage applied to the gate nodeInput LineLocation on a device where the signal is inputInput NetworkGroup of electronic components associated with the input of a deviceInput SignalSignal input to an electronic componentIsolating Said DC Bias Signal From All But Said Selected One of Said PluralityThe applied DC bias is separated electrically from all amplifier stages except the selected one of Other Amplifier Stages | |
|--|-------|
| to the drain node is controlled by an electric field caused by a voltage applied to the gate nodeInput LineLocation on a device where the signal is inputInput NetworkGroup of electronic components associated with the input of a deviceInput SignalSignal input to an electronic componentIsolating Said DC Bias Signal From All But Said Selected One of Said Plurality stages except the selected one | node |
| voltage applied to the gate nodeInput LineLocation on a device where the signal is inputInput NetworkGroup of electronic components associated with the input of a deviceInput SignalSignal input to an electronic componentIsolating Said DC Bias Signal From All But Said Selected One of Said Plurality stages except the selected one | |
| Input LineLocation on a device where the signal is inputInput NetworkGroup of electronic components associated with the input of a deviceInput SignalSignal input to an electronic componentIsolating Said DC Bias Signal From All But Said Selected One of Said Plurality stages except the selected one | |
| Input Network Group of electronic components associated with the input of a device Input Signal Signal input to an electronic component Isolating Said DC Bias Signal From All The applied DC bias is separated electrically from all amplifier But Said Selected One of Said Plurality stages except the selected one | |
| deviceInput SignalSignal input to an electronic componentIsolating Said DC Bias Signal From AllThe applied DC bias is separated electrically from all amplifierBut Said Selected One of Said Plurality stages except the selected one | |
| Input SignalSignal input to an electronic componentIsolating Said DC Bias Signal From All The applied DC bias is separated electrically from all amplifierBut Said Selected One of Said Plurality stages except the selected one | |
| Isolating Said DC Bias Signal From All The applied DC bias is separated electrically from all amplifier But Said Selected One of Said Plurality stages except the selected one | |
| But Said Selected One of Said Plurality stages except the selected one | |
| | 1 |
| of Other Amplifier Stages | |
| of Other Amplifier Stages | |
| Node Location where one or more signals is input and one or more sig | gnals |
| is output | |
| Output Network Group of electronic components associated with the output of a | |
| device | |
| Output Node A node (location where one or more signals is input and one or | |
| more signals is output) whose output is the output of the reference | ced |
| circuit | |
| Plurality Two or more | |
| Radio Frequency (RF) Frequency useful for radio communication | |
| Selected Amplifier Stages Multiple stages that are selected | |
| Selecting Particular Amplifier Stages Selecting more than one amplifier stage | |
| SignalInformation that can be transmitted or received within a circuit | |
| Signal BoundariesBorder or transition between the digital words or symbols in a | |
| signal | |
| Successive Portions Limited parts that follow each other in order | |
| Timing Information Input Line An electrical line that receives information that represents the | |
| Receiving Timing Information periods during which there are boundaries in the RF input signal | 1 |
| Representative of the Boundaries | |
| Between the Portions of the RF Input | |
| Signal | |
| Timing Information Representative of Information that represents the periods during which there are | |
| the Boundaries Between the Portions of boundaries in the RF input signal | |
| the RF Input Signal | |
| Words A set number of data symbols or characters transmitted together | as |
| a group | |

S.D.Cal.,2004. Qualcomm Inc. v. Conexant Systems, Inc.

Produced by Sans Paper, LLC.