United States District Court, E.D. Virginia, Alexandria Division.

HARRIS CORPORATION and Harris Semiconductor Patents, Inc,

Plaintiffs. v. **ATMEL CORPORATION,** Defendant.

C.A. No. 98-98-A

Aug. 3, 1998.

In suit alleging infringement of patent for process for forming contoured openings in insulating layers of semiconductor devices, parties filed cross motions for summary judgment. The District Court, Ellis, J., held that: (1) second heating or partial reflow step of patent was not literally infringed; (2) summary judgment in favor of defendant on issue of infringement under doctrine of equivalents was precluded by fact issues; and (3) fact issue precluded summary judgment in favor of plaintiff.

Defendant's motion granted in part and denied in part; plaintiff's motion denied.

4,349,584. Cited.

John F. Anderson, Richards McGettigan Reilly & West, P.C., Alexandria, VA, Michael E. Dergosits, Todd A. Noah, Dergosits & Noah, L.L.P., Henry C. Bunsow, Keker & Van Nest, L.L.P., San Francisco, CA, for Plaintiffs.

Charles D. Ossola, Timothy R. DeWitt, Arnold & Porter, Washington, DC (Robert Haslam, Keith R. Weed, Nitin Subhedar, Heller Ehrman White & McAuliffe, Palo Alto, CA, Michael K. Plimak, Heller Ehrman White & McAuliffe, San Francisco, CA, of counsel), for Defendant.

MEMORANDUM OPINION

ELLIS, District Judge.

Harris' FN1 United States Patent No. 4,349,584 ("the '584 patent") is one of eight semiconductor patents at issue in this litigation. Now before the Court are the parties' cross motions for summary judgment on the subject of infringement of the '584 patent. At issue, essentially, is the proper construction of two disputed terms within claim 1 of the patent, and, of course, a determination of whether these terms, properly construed, read on the accused process. For the reasons that follow, summary judgment of non-infringement must be granted as to literal infringement of the '584 patent, but denied as to infringement under the doctrine of equivalents.

FN1. Plaintiff Harris Semiconductor Patents, Inc. (hereinafter "Harris"), is the sole owner of the '584 patent.

The '584 patent, titled "Process for Tapering Openings in Ternary Glass Coatings," relates generally to a method for fabricating semiconductor devices, and, more particularly, to a process for forming contoured openings in insulating layers of semiconductor devices. It is the latter process that lies at the heart of the invention claimed in the '584 patent, and which is central to the disputes at bar. But, to begin with, it is useful as context to describe briefly the typical process steps involved in manufacturing a semiconductor device, at least to the extent those steps are relevant to the '584 patent.

Semiconductor devices are made by placing successive layers of various materials on a substrate base. During the layering process, particular layers may be removed altogether, or, etched using a template (otherwise known as a mask) to form a pattern, thereby leaving portions in place. This process of layering, removing, and etching is repeated until the desired structure is achieved in the semiconductor material. And, after the desired structure is achieved, but before depositing a first metal layer to connect the semiconductor devices electrically, an insulating, *i.e.* non-conductive, layer of material is deposited on the semiconductor body. This insulating layer is critical, as it protects the conductive structures of the semiconductor device.

The insulating material, typically a silicon oxide, can be applied by depositing the material on the surface of the semiconductor and then heating the entire device to a sufficient temperature and for a sufficient time to allow the deposited material to flow over the entire surface of the device to create a relatively smooth surface.FN2 The temperature required to flow the insulating material depends, in part, on the material's characteristics. For example, adding various impurities, such as phosphorous, boron, or a combination of both, to the silicon oxide through a process called doping will allow the oxide to flow at lower temperatures than if a pure silicon oxide is used. Moreover, changing the concentrations of boron and phosphorous in the silicon oxide doped with combinations of boron and phosphorous, a substance known as BPSG FN4, is particularly suitable to the semiconductor fabrication process because of the lower temperatures at which this insulating material flows.

FN2. This method for applying the insulating material is referred to as "chemical vapor deposition."

FN3. Changing the concentration levels of boron and phosphorous provides only one of the variables that will affect the temperature at which the insulating material will flow across the semiconductor. A second variable is, of course, the amount of time the material is exposed to a certain temperature. And, a third factor that affects the flow temperature is the ambient gas atmosphere in which the material is heated.

FN4. BPSG stands for "borophosphosilicate glass," commonly called a "ternary glass" because it has three separate components: oxides of boron, phosphorous, and silicon.

After the BPSG insulating layer is applied, contact holes must be cut through the BPSG layer to expose the conductive structures that lie below the insulation. This is accomplished by placing a mask template on the formed BPSG layer, after which contact holes are cut using one of two methods: wet etching or reactive plasma etching.FN5 Difficulties are associated with both methods. If a wet etch is used to cut the contact holes, it is difficult to control the shape and dimensions of the holes. If a reactive plasma etch is used, the walls of the contact holes can be made essentially vertical. Both etching methods can thus result in sharp or abrupt edges that, in turn, cause discontinuities when subsequent layers are deposited. These discontinuities can result in malfunctions, and inoperative devices.

FN5. With "wet etching", chemicals are applied to remove those portions of the insulating layer that are exposed through the mask template. The type and the strength of the chemicals used as well as the length of

time that the chemicals are left on the surface determine the amount of material that is etched away. "Reactive plasma etching" is performed by bombarding the portions of the layer not covered by the mask template with ions and molecules to remove desired portions of the layer.

In essence, the '584 patent discloses a method that alleviates the problems arising from the abrupt edges that result from etching contact holes in the insulating layer. Specifically, the '584 patent teaches a second heating or partial reflow step, which softens the BPSG after the contact holes are formed. This partial reflow step contours the contact hole edges prior to the deposition of the metal layer, yielding improved metal connection in the contact hole while controlling the hole dimensions. Thus, the method teaches the use of lower temperatures during the partial reflow step to prevent a second full flow of the BPSG, and to prevent the formation of significant, undesirable oxide growth within the contact hole. Such growth might offset any improved contact gains made by the reflow process.

Claim 1 of the '584 patent, the only claim which is pertinent to the parties' cross motions FN6, reads, as follows:

FN6. Claims 2-8 of the '584 patent are dependent on Claim 1.

1. A process for forming a tapered opening in a glass passivating coating on the surface of a semiconductor body comprising the steps of:

forming a layer of dense, undoped silicon oxide on the semiconductor body;

forming a layer of ternary doped silicon oxide on the undoped layer, the doped layer characterized by having a given flow temperature;

forming a contact opening in both the silicon oxide layers to expose a portion of the semiconductor body; and

heating both oxide layers to a temperature below the given flow temperature of the doped layer for a period of time sufficient to only soften and partially reflow the doped layer at the edges of the contact opening yet insufficient to form a significant oxide growth on the exposed portion of the semiconductor body.

In the instant case, Harris contends that defendant Atmel Corporation, in fabricating several of the accused semiconductor products FN7, infringes the process steps claimed in the '584 patent. Atmel concedes that the fabrication process in issue FN8, which also involves tapering the contact openings in the BPSG layer of semiconductors, performs the first three steps claimed in the '584 patent. Thus, the accused Atmel process (i) forms a layer of undoped silicon oxide on the semiconductor body, (ii) forms a layer of ternary doped silicon oxide on the undoped layer, and (iii) forms contact openings in both silicon oxide layers. All that is at issue then is whether the accused process infringes the fourth step claimed in the '584 patent, the reheating or partial reflow step.

FN7. Harris has identified Atmel products AT29C256-15PC (256K Flash) and AT28LV64B-25TC (64K parallel EEPROM) as made using the patented process.

FN8. It is worth noting that the process discussed here is not Atmel's new Tungsten Plug fabrication process, but rather the older "AT19003" process. Atmel's new Tungsten Plug process is no longer in issue in this litigation.

In this regard, Atmel contends that the accused process cannot infringe the '584 patent because during the partial reflow step, the accused process (1) heats the oxide layers to a temperature above the "given flow temperature," and (2) creates significant oxide growth in the contact holes.FN9 In response, Harris contends that the '584 patent is not restricted to processes in which the absolute temperature during the partial reflow step is below the absolute flow temperature measured during the initial deposition of the BPSG layer. Rather, Harris contends that the patent requires only that during the second heating step, the BPSG layer be heated to a temperature below the flow temperature for the particular conditions, including time of heating and the nature of the ambient atmosphere, existing during the second heating. Further, Harris contends that the parties' cross motions for summary judgment thus requires construction of the terms "given flow temperature" and "significant oxide growth," and, of course, a determination of whether these terms, properly construed, read on the accused process.

FN9. Atmel contends that the creation of significant oxide growth during its partial reflow step is evidenced by the separate etch that must be performed to remove the oxide growth from the contact hole.

II.

Summary judgment is appropriate where the "pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to judgment as a matter of law." Rule 56(c), Fed.R.Civ.P. Nor is there any doubt that this standard is equally applicable in patent infringement actions. *See* Johnston v. IVAC Corp., 885 F.2d 1574, 1576-77 (Fed.Cir.1989).

[1] [2] [3] Specifically, literal infringement is determined by a two-step analysis: (1) First, claim construction to determine what the claims cover, *i.e.*, their scope, followed by (2) a determination of whether the properly construed claims read on the accused structure or process. *See* Markman v. Westview Instruments, Inc., 52 F.3d 967, 976 (Fed.Cir.1995). Now firmly settled is the principle that the first step in the analysis, claim construction, is exclusively within the province of the Court. *See* id. at 979. Thus, where the "parties do not dispute any relevant facts regarding the accused product but disagree over which of two possible meanings of [the relevant claim] is the proper one, the question of literal infringement collapses to one of claim construction and is...amenable to summary judgment." Athletic Alternatives, Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1578 (Fed.Cir.1996).

[4] Also now clear is that in interpreting an asserted claim, the district court "should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996) (citing Markman, 52 F.3d at 979). Such intrinsic evidence is "the most significant source of the legally operative meaning of disputed claim language." *Id*.

[5] [6] [7] [8] Thus, the claim construction enterprise properly begins with an examination of the words of the claims themselves, both asserted and nonasserted, to determine the scope of the patented invention. *See id.* (citing Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 620 (Fed.Cir.1995)). And typically, such words should be given their plain and ordinary meaning. *See id.* However, a patentee "may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patente has used any terms in a manner inconsistent with their plain and ordinary meaning. *See id.* As the Federal Circuit has repeatedly stated, "claims must be read in view of the specification, of which they are a part." *Id.* (quoting Markman, 52 F.3d at 979).FN10 Yet, while it is fundamental that claims are to be construed in light of the

specification, courts must avoid incorporating limitations found only within the specification into the claim itself. *See* Transmatic, Inc. v. Gulton Indus. Inc., 53 F.3d 1270, 1277 (Fed.Cir.1995) (limitations unique to preferred embodiments of the invention do not restrict the scope of the claimed invention). Finally, courts may consider the prosecution history of the patent, provided it is in evidence. *See* Vitronics, 90 F.3d at 1582.

FN10. Indeed, in emphasizing the significance of the specification to the claim construction process, the Federal Circuit has said that:

The specification contains a written description of the invention which must be clear and complete enough to enable those of ordinary skill in the art to make and use it. Thus, the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.

See Vitronics, 90 F.3d at 1582.

[9] Where, as here, the intrinsic evidence of record unambiguously describes the scope of the patented invention, the claim construction process is at an end. *See* id. at 1583. In such circumstances, reliance on any extrinsic evidence to resolve the meaning of the disputed claim is improper. *See id*.FN11

FN11. In the instant case, as in most such cases, the parties rely to varying degrees on expert reports submitted in support of their motions for summary judgment. Because such reports fall squarely within the category of extrinsic evidence, their role in the claim construction process is limited. Specifically, such reports are consulted and relied on only to the extent that they help explain the technology underlying the patented product or process, and the specific claims at issue. Such reports are not entitled to weight to the extent that they advocate a position concerning the meaning of claim language. *See, e.g.*, Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1578 (Fed.Cir.1995).

III.

A. " Given Flow Temperature "

[10] The meaning of the disputed term "given flow temperature," used twice in claim 1 of the '584 patent, is clear from a reading of the claim itself and the patent specification. Specifically, it is the temperature at which a particular ternary doped silicon oxide, heated for a specific period of time, and in a given atmosphere, will flow across the semiconductor body to form the insulating layer.FN12 As such, the "given flow temperature" for a particular layer is a definite, quantifiable temperature which serves as the key reference point in the two heating steps FN13 described in the patent. First, the ternary doped silicon oxide layer must be heated to the "given flow temperature" so that it will flow over the semiconductor body and create an insulating layer with a relatively smooth surface. Second, and after forming the contact holes, the ternary doped silicon oxide layer must be reheated to some temperature "below the given flow temperature" to soften, and only partially reflow the layer at the edges of the contact holes.

FN12. For example, the specification notes that a BPSG layer having about 3-3 1/2 wt % phosphorus and about 2-2 1/2 wt % boron will flow when heated to about 900 (deg.) C, in steam, for a period of about 30 minutes. If heated in helium, nitrogen, argon, or some other inert atmosphere, however, this BPSG will flow when heated to about 950 (deg.) > C for 30 minutes. Similarly, a BPSG layer having about 4-5 wt % phosphorus and about 3-4 wt % boron will flow when heated to about 800 (deg.) > C in steam, and about 850 (deg.) C when heated in helium, nitrogen, argon, or some other inert atmosphere. *See* '584 patent, col. 2, ll. 55-68; col. 3, ll. 5-11.

In light of this construction, and the evidence regarding Atmel's accused process, it is also clear that claim 1 of the '584 patent is not literally infringed. In forming a layer of ternary doped silicon oxide on the Atmel semiconductors, the accused process flows the deposited BPSG over the surface of the device by heating it to a temperature of 890 (deg.) C, the BPSG's given flow temperature. Then, after the contact openings are formed, the BPSG layer is rapidly and very briefly reheated to a temperature of 910 (deg.) C to soften and partially reflow the BPSG layer at the edges of the contact holes. Thus, because the accused process does not heat the insulating layer "to a temperature below the given flow temperature" during the partial reflow step, a limitation found in claim 1 of the '584 patent, claim 1 of the '584 patent is not literally infringed. '584 patent, col. 4, ll. 21-22.

Harris's arguments made in an effort to avoid this result are unavailing. Essentially, Harris contends that the "given flow temperature" of the doped layer, as defined in the second step of the '584 patent, need not be the same and may be lower than the "given flow temperature" of the doped layer in the fourth step of the patent, depending upon the conditions present in the two separate heating steps. Thus, Harris argues that the '584 patent may be infringed by a tapering process that heats the doped layer during the second heating or partial reflow step to a temperature higher than the temperature of the doped layer at which it flows during the initial heating step. Yet, this argument ignores the clear connection between the two heating steps-the initial flow of the doped layer and the partial reflow of the doped layer-as described in the patent. In the first heating step, the doped layer is "characterized by having a given flow temperature", and in the second heating step, the doped layer is heated "to a temperature below the given flow temperature." It seems clear that the claim's second use of the term "given flow temperature" must be interpreted as an explicit reference to the first. Cf. Southwall Technologies, 54 F.3d at 1579 (the same term used in several claims must be interpreted consistently in all claims). Moreover, to give the word "below" any meaning, there must be some reference temperature, and in claim 1 of the '584 patent, that reference temperature is plainly the temperature at which the doped layer was initially made to flow across the semiconductor, namely the "given flow temperature." Thus, because the accused process does not reheat the doped layer during the partial reflow step "to a temperature below the given flow temperature," this element of the '584 patent is not literally infringed.

[11] [12] [13] Although the absence of this limitation from the accused process precludes literal infringement, there may still be infringement under the doctrine of equivalents, which prevents an accused infringer from avoiding infringement altogether by "changing only minor or insubstantial details of a claimed invention while retaining their essential functionality." Sage Prods., Inc. v. Devon Indus., Inc., 126 F.3d 1420, 1424 (Fed.Cir.1997). The essential doctrine of equivalents inquiry is whether the "accused product or process contain[s] elements identical or equivalent to each claimed element of the patented invention." Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co., 520 U.S. 17, 117 S.Ct. 1040, 1054, 137 L.Ed.2d 146 (1997). Thus, the proper focus is on the individual elements of the claimed invention, and in particular, determining whether a substitute element "matches the function, way, and result of the claimed element." *Id.* And, while equivalence is a factual matter normally reserved for a fact finder, summary judgment is appropriate where no reasonable fact finder could find equivalence. *See* Sage Prods., 126 F.3d at 1423.

[14] [15] Harris contends that even if there is no literal infringement, the partial reflow step in the accused process nonetheless performs the same function in the same way to achieve the same result as the patented invention; it heats the ternary doped layer sufficient only to soften and partially reflow the doped layer to form tapered edges at the contact openings. And significantly, Atmel concedes that new technology-technology not available in 1982 when the '584 patent issued-is used to heat the BPSG layer during the partial reflow step. While courts must generally exercise "special vigilance against allowing the concept of equivalence to eliminate completely" any of the individual elements of the claimed invention,FN14 the doctrine of equivalents prevents an infringer from avoiding a patent by using later-developed technology to

create a variant in the invention that "constitute[s] so insubstantial a change from what is claimed in the patent" that it should be deemed an infringing product. Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc., 145 F.3d 1303, 1310 (Fed.Cir.1998); *see also* Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 938 (Fed.Cir.1987) ("[T]he facts here do not involve later-developed computer technology which should be deemed within the scope of the claims to avoid the pirating of an invention."). These principles, given the current record, preclude summary judgment on the issue of infringement under the doctrine of equivalents.

FN14. See Warner-Jenkinson, 117 S.Ct. at 1054.

B. " Significant Oxide Growth "

[16] As a separate claim element, the '584 patent cautions that the temperature and time of heating used during the partial reflow step must be "insufficient to form a significant oxide growth on the exposed portion of the semiconductor body." The term "significant oxide growth" is not defined within the claims, nor is it a term that has a generally accepted meaning independent of the patent. Nevertheless, a review of the specification and the background to the invention reveals the proper scope of this disputed term.

As the patent makes clear, the partial reflow step that is central to the claimed invention is designed to improve metal connection within the semiconductor by tapering the edges of a formed contact hole while otherwise maintaining the essential integrity of the hole. Yet, reheating may inevitably result in some new oxide formation within the contact hole, which if significant, could defeat the purpose of the partial reflow step. Thus, the patent teaches that the temperature and heating time during the reflow step must be such that any formation of oxide growth "will be so thin that any subsequent deposition of a metallic interconnect thereon will readily punch through and provide good contact to the surface of the silicon." '584 patent, col. 3, ll. 50-53. It follows from this passage that the meaning of the disputed term "significant oxide growth" is a thickness of oxide growth that a metallic interconnect will not readily punch through when deposited thereon.

Yet, this interpretation does not end the claim construction process, for although the specification suggests that a separate etching step will not be necessary to remove any oxide growth that has formed, the claims of the patent do not preclude such a step. Rather, the patent merely describes the potential disadvantage of a separate etching. Specifically, etching to remove the undesirable oxide that has formed during the reflow step may also remove the desirable oxide from the insulating layer, and thereby disrupt the integrity of the hole. It is this complication associated with a separate etching step, and not the step itself, which must be avoided under the '584 patent. Thus, an alternative definition of "significant oxide growth" is a thickness of oxide growth that requires removal by a separate etching step that will simultaneously remove desirable oxide and thereby disrupt the integrity of the contact hole. Thus, the term "significant oxide growth" is properly defined in full, as follows:

A thickness of oxide growth on the exposed portion of the semiconductor body (1) that a metallic interconnect will not readily punch through when deposited thereon, or (2) that requires removal by a separate etching step that will simultaneously remove desirable oxide and thereby disrupt the integrity of the contact hole.

And, in the instant case, while Atmel performs a separate etching to remove the oxide formed during the reflow step, the record does not disclose (1) whether a metallic interconnect would readily punch through that oxide layer were it not removed, nor (2) whether the separate etching removes desirable oxide and thereby disrupts the integrity of the contact hole. Accordingly, it is unclear whether the temperature utilized in the accused process is "insufficient to form significant oxide growth," and hence whether the accused process infringes this element either literally or under the doctrine of equivalents.

IV.

For the reasons here stated, Atmel's motion for summary judgment of non-infringement must be granted as to literal infringement of the '584 patent, but denied as to infringement under the doctrine of equivalents. Harris's cross motion for summary judgment of infringement of the '584 patent must be denied.

An appropriate order shall enter.

E.D.Va.,1998. Harris Corp. v. Atmel Corp.

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