United States District Court,
D. Delaware.

THORN EMI NORTH AMERICA, INCORPORATED,
Plaintiff.
v.
INTEL CORPORATION,
Defendant.

Civil Action No. 95-199-RRM

May 28, 1996.

Patentee brought infringement action against competitor, alleging infringement of its patent for improved method of fabricating metal oxide semiconductor (MOS) field effect transistors in large scale integrated circuits. On competitor's motion for partial summary judgment, the District Court, McKelvie, J., held that: (1) patent required doping of gate electrode wired to differentially growing dielectric implant mask, and (2) competitor's processes were not infringing.

Judgment for competitor.

4,486,394. Not infringed.

Josy W. Ingersoll, Martin S. Lessner, Lisa B. Goodman, Young, Conaway, Stargatt & Taylor, Wilmington, Delaware; Donald F. Parsons, Jr., Lisa B. Baeurle, Morris, Nichols, Arsht & Tunnell, Wilmington, Delaware; James P. Bradley, Dale B. Nixon, Michael Rocco Cannatti, D. Scott Hemingway, Michael Chibib, Richards, Medlock & Andrews, Dallas, Texas; Ivan S. Kavrukov, Peter J. Philips, Cooper & Dunham, L.L.P., New York City, for plaintiff Thorn EMI North America, Inc.

William J. Marsden, Jr., Joanne Ceballos, Potter, Anderson & Corroon, Wilmington, Delaware; James J. Elacqua, Timothy N. Trop, Christopher R. Benson, Stephen D. Dellett, Henry A. Petri, Jr., Arnold, White & Durkee, Houston, Texas, for defendant Intel Corporation.

McKELVIE**, District Judge.**

This is a patent case. Plaintiff Thorn EMI North America, Inc. ("TENA") is the owner of U.S. Patent No. 4,486,943 ("the "3 patent"). The "3 patent claims an improved method for fabricating metal oxide semiconductor ("MOS") field effect transistors in a large scale integrated circuit. On March 29, 1995, TENA filed a complaint against defendant Intel Corporation ("Intel") alleging infringement of the "3 patent. On November 14, 1995, Intel filed a motion for partial summary judgment that Intel processes P652 and P852 (revisions 9 and 10) do not infringe the "3 patent. This is the court's decision on Intel's motion.

I. *FACTUAL AND PROCEDURAL BACKGROUND*

On January 31, 1996, the court held an oral argument on Intel's motion for partial summary judgment. The court draws the following facts from the "3 patent claims and specification, the prosecution history of the "3 patent, the briefs of the parties submitted in connection with Intel's motion, the declarations of Dr. Fair, TENA's expert, and Dr. Chung, Intel's expert, and the oral argument.

A. *The Basic Technology Underlying This Lawsuit*

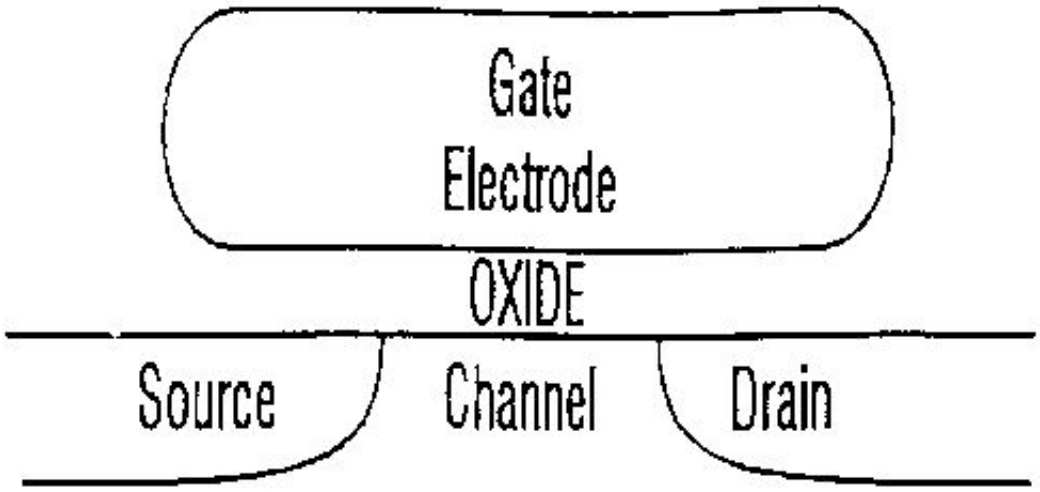
MOS field effect transistors, or simply MOS transistors, are devices found on integrated circuit computer chips, such as static random access memory chips ("SRAMs") and microprocessor chips. A typical microprocessor chip contains anywhere from several hundred thousand to several million MOS transistors. Each MOS transistor generates a signal by acting as a switch that can selectively turn on or off an electrical current. The signals generated by the MOS transistors on an integrated circuit chip control the operations of the computer.

1. *The structure of an MOS transistor*

An MOS transistor generally consists of the following sections. First, there is the "substrate," which is the bottom layer of the transistor. The substrate is formed from a material, such as monocrystalline silicon, that is a poor conductor. Monocrystalline silicon is essentially a wafer of very pure glass made of a tightly packed and neatly organized single-crystal structure. Second, there is a "source" region at one end of the substrate and a "drain" region at the other end. The source and drain regions are areas of electrical conductivity that are formed by a process known as "doping." Doping involves implanting certain types of ions into the substrate. These ions, which are sometimes referred to simply as impurities, essentially "rain" down onto the ends of the substrate where they become embedded.

Third, there is a "gate electrode" formed on top of the substrate between the source and drain regions of the substrate. The gate electrode may be formed either from a conductive material, such as a metal, or a nonconductive material, such as polysilicon. Polysilicon is made of loosely packed, minute pieces of silicon oriented differently from each other. If polysilicon is used, it also must be doped to become electrically conductive. Finally, the gate electrode is separated from the substrate by a relatively thin "dielectric,"which is a material that does not conduct electricity. For example, a thin layer of oxide may separate the gate electrode and the substrate.

The following illustration demonstrates the various parts of an MOS transistor.



The name "metal oxide semiconductor" field effect transistor derives from the use of a metal gate electrode on top of the substrate, an insulating oxide layer between the gate electrode and the substrate, and a substrate made from a semiconductive material. However, the term "MOS field effect transistor" now refers to any transistor that has a conductive gate electrode on top of a semiconductive substrate with a layer of dielectric insulating the gate electrode from the substrate. For example, some of the MOS transistors manufactured by the processes claimed in the "3 patent do not require the use of a metal gate electrode or an insulating oxide layer.

2. ***The operation of an MOS transistor***

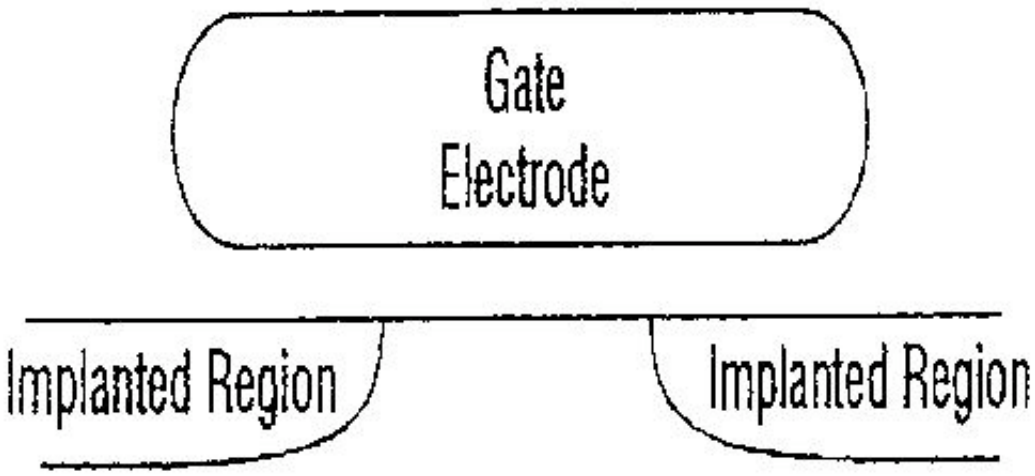
MOS transistors operate in the following manner. When a voltage is applied to the gate electrode on top of the substrate, a channel opens between the source and drain regions within the substrate. This allows a current to flow through the transistor, between the source and drain regions and underneath the gate electrode. This current generates a signal that is communicated to various portions of a computer in combination with the signals from other MOS transistors on the integrated circuit chip. When the voltage is turned off, the transistor ceases to generate the signal.

3. ***Manufacturing processes for MOS transistors before*** the "3 patent

Conventional processes for manufacturing MOS transistors before the issuance of the "3 patent involved starting with a substrate, forming an insulating dielectric on the substrate, forming a gate electrode on top of the insulating layer, doping the substrate to create the source and drain regions, and then heating the transistor. The heating is necessary to "activate" the source and drain regions, in other words, to give those areas the property of electrical conductivity. An incidental consequence of the heating step is that the ions, or impurities, in the substrate are driven deeper into the substrate and farther towards the center of the substrate. Those skilled in the art of making MOS transistors refer to this heating step as "heat driving" the source and drain regions. The movement of the source and drain regions toward the center of the substrate is referred to as "lateral diffusion."

Using conventional techniques known before the issuance of the "3 patent, each of these steps could be done in various ways. For example, the insulating dielectric could be deposited on top of the substrate, or it could be "grown" by heating the substrate in an oxygen oven. During the heating process, the top surface of the substrate is converted into another material, such as oxide, in a manner similar to the way that metal rusts. In addition, the gate electrode could be deposited just in the middle on top of the substrate, or it could be deposited along the entire surface of the substrate and etched to remove the unnecessary portions. Finally, the gate electrode could be doped prior to the doping of the substrate, or it could be doped at the same time as the substrate.

A problem existed with these conventional techniques, however. When the source and drain regions were implanted, the edges of these regions were aligned vertically with the edges of the gate electrode before heat driving. Then the heat driving step would cause the source and drain regions to diffuse laterally underneath the gate electrode.



This "overlap" between the edges of the source and drain regions and the gate electrode caused something known in the field as "Miller capacitances." Miller capacitances reduce the operating speed of the transistor, which is an undesirable result because the speed of a transistor is the key to its functionality and commercial desirability. Ideally, to prevent the occurrence of Miller capacitances, the edges of the source and drain regions should be aligned vertically with the edges of the gate electrode *after* heat driving, rather than before.

To solve this problem, some of those skilled in the art of making MOS transistors proposed establishing a dielectric or a "photoresist" layer on top of the gate electrode material, then undercutting the gate electrode, which would leave an overhang of the dielectric or photoresist layer over the gate electrode. A photoresistive material is a material whose conductivity is affected by light or other radiation. The overhang existed to prevent implantation of the source and drain regions right next to the gate electrode. Therefore, the edges of the source and drain regions would be separated laterally from the edges of the gate electrode.

Then the heat driving step would laterally diffuse the source and drain regions until those regions were aligned vertically with the edges of the gate electrode, thus leaving no overlap. In practice, however, the undercut was difficult to control, and vertical alignment between the gate electrode and the source and drain regions fluctuated significantly.

B. *The* "3 Patent

The "3 patent claims an improved process for fabricating MOS transistors to reduce Miller capacitances and increase operating speed. The patent has four independent claims, 1, 6, 10, and 15, and fourteen dependent claims, 2-5, 7-9, 11-14, and 16-18. TENA is only asserting independent claims 1, 6, and 15, and dependent claims 2, 3, 16, and 17. However, independent claim 10 is relevant to the parties' claim construction arguments.

1. *The claims of* the "3 patent

Independent claim 1 reads as follows:

1. A method of fabricating on a substrate an MOS transistor having a gate electrode and a self-aligned source/drain region with zero overlap comprising:

(a) forming a doped polysilicon gate electrode upon but insulated from the substrate; then

(b) differentially thermally growing an oxide to serve as an implant mask having controlled thickness on both the top and sides of the gate electrode whereby a relatively thicker layer of oxide is developed on the top and sides of the gate electrode and a relatively thinner layer of oxide is developed on the intended source and drain regions of the substrate; then

(c) anisotropically etching said oxide;

(d) implanting a source/drain region in the substrate such that said implant mask shields an underlying portion of the substrate from implantation to result in a gap between a side edge of the gate electrode and a side edge of the implanted region; and then

(e) heat driving the implanted source/drain region until its side edge is substantially aligned with the previously separated side edge of the gate electrode, whereby the source/drain edge is aligned with the gate electrode edge and there is substantially zero overlap.

Anisotropic etching, mentioned in step (c) of claim 1, refers to the process of removing surface material in different directions at different rates, as opposed to isotropic etching, which involves removing surface material in all directions at the same rate. The role of anisotropic etching will become clear below in discussing the preferred embodiment of the "3 patent. The language of dependent claims 2 and 3, although asserted by TENA, is not relevant to Intel's motion.

Independent claim 6 reads as follows:

6. A method of fabricating on a substrate an MOS transistor having a gate electrode and a self-aligned source/drain region comprising:

(a) forming a doped polysilicon gate electrode insulated from the substrate;

(b) growing a dielectric layer over the gate electrode by a process controlled to develop a high differential of dielectric thickness such that the dielectric is relatively thick over the top and sides of the gate electrode and relatively thinner over the intended source/drain regions;

(c) anisotropically etching said dielectric layer;

(d) implanting the source/drain region such that its edge is laterally offset from the substrate area below the gate electrode due to said dielectric layer being present on the sides of the gate electrode;

(e) heat driving the source/drain region laterally until its edge is substantially vertically aligned with the side of the gate electrode;

(f) etching contact area to expose a part of the source/drain region and yet maintaining the dielectric on the top and sides of the gate electrode; and

(g) forming a conductive contact in the etched area, wherein the source/drain region is properly aligned with the gate electrode and the conductive contact is aligned with the source/drain region without shorting the gate electrode.

Steps (f) and (g) relate to forming contact areas on top of the transistor, which part of the process is not directly relevant to this litigation. However, these steps will assist in interpreting the language used in earlier steps of the entire process outlined in claim 6.

Independent claim 10, which TENA originally asserted in this litigation but ultimately withdrew, reads as follows in relevant part:

10. A method of fabricating a self-aligned semiconductor device having a gate, a source, and a drain with zero overlap comprising:

(a) forming a defined gate electrode insulated from and over a substrate, said gate electrode being polysilicon which is doped to promote a high rate of differential thermal oxidation, said substrate being monocrystalline silicon; then

(b) establishing an isolating oxide layer on the top and sides of said gate electrode by thermal oxidation under ambient conditions controlled such that the oxide layer covers the top and sides of the gate electrodeand regions in the substrate where the source and drain will be formed, the oxide growing substantially thicker on the top and sides of the gate electrode than above the prospective source and drain;

....

Independent claim 15 reads as follows:

15. A method of fabricating on a substrate an MOS transistor having a gate electrode and a self-aligned source/drain region with zero overlap comprising:

[(a)] forming a doped gate electrode insulated from the substrate, said substrate being monocrystalline silicon; then

[(b)] establishing an isolating oxide on the top and sides of the gate electrode and over the substrate adjacent the gate electrode such that the oxide on the top and sides of the gate electrode is relatively thick compared to the oxide over the substrate, including oxidizing in a steam atmosphere at a temperature which promotes high differential rates of growth of oxide as between the doped poly gate electrode and the substrate;

[(c)] anisotropically etching the oxide at the top of the gate electrode and the intended source/drain region to leave oxide on at least the sides of the gate electrode;

[(d)] implanting a source/drain region in the substrate so that the oxide on the sides of the gate shield the underlying portion of the substrate from implantation thereby to provide a gap between a side edge of the gate electrode and side edge of the implanted region; then

[(e)] heat driving said implanted source/drain region so that its side edge can be substantially aligned with the previously separated side edge of the gate electrode and no substantial gap or overlap exists between the source/drain region and the gate electrode.

Dependent claim 16 reads as follows:

16. A method as set forth in claim 15 wherein the source/drain region is implanted while the top of the gate electrode is substantially free of dielectric for doping the gate electrode during source/drain implantation.

Dependent claim 17 reads as follows:

17. A method as set forth in claim 15 wherein a relatively thin oxide is formed over the gate electrode, the dielectric remnants and the intended source/drain region prior to implantation.

By definition, dependent claims 16 and 17 contain all of the limitations of independent claim 15. *See* 35 U.S.C. s. 112.

2. *The preferred embodiment of* the "3 patent

The specification sets out the preferred embodiment of the invention claimed in the "3 patent. First, a layer of oxide is formed upon a substrate. Second, a doped polysilicon layer is defined and etched on top of the layer of oxide to form a gate electrode. Third, a dielectric layer, such as oxide, is grown on top of the gate electrode and the substrate by steam oxidation at 850 (deg.)C. The resulting oxide layer "on the top and sides of the gate electrode is relatively thick compared to the oxide layer adjacent the gate electrode over the intended source/drain regions." For example, the thickness of oxide over the top and sides of the gate electrode is 500 nanometers, whereas the thickness over the substrate is 170 nanometers. This varying thickness occurs "because the oxide grows faster over the top and sides of the doped gate electrode." This third step is called "differential thermal growth" in the patent.

Figure 1 from the "3 patent illustrates the result of these first three steps, where 10 is the substrate, 14 is the insulating layer of dielectric, 16 is the doped gate electrode, 18 is the differentially grown oxide layer, and

2Q(20) and 22 are the source and drain regions.

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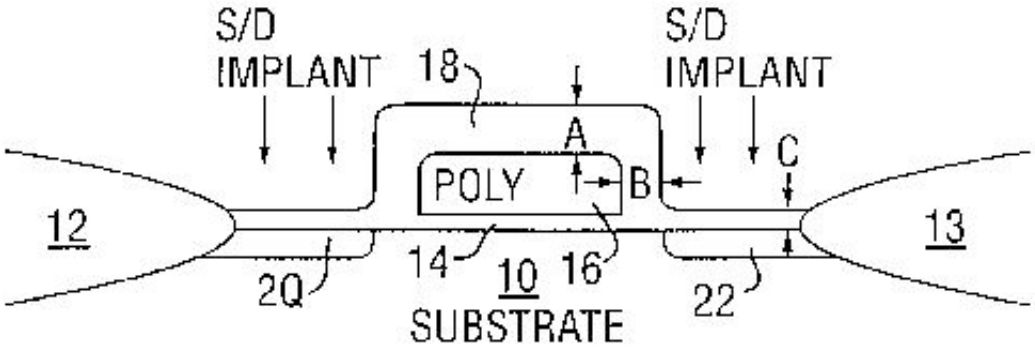

FIG. 1

Fourth, source/drain regions are implanted with arsenic or phosphorous ions. During this fourth stage, the differentially thermally grown oxide layer serves as an "implant mask" to prevent these impurities from being implanted next to the gate electrode:

Because of the masking effect provided by the oxide on the sides of the gate electrode, the source/drain regions are not implanted adjacent to the vertical edges of the gate electrode. Rather, a gap is provided between the gate electrode and the source/drain regions to allow for subsequent diffusion of the source/drain regions.

Fifth, the source/drain regions are heat driven into the substrate until the edges of the regions are substantially vertically aligned with the edges of the gate electrode. After this heat treatment, certain additional steps are performed to form contact regions. These process steps are not relevant to the present litigation.

Figure 2 from the "3 patent illustrates the result of these remaining steps, where the source and drain regions (2Q (20) and 22) are substantially vertically aligned with the edges of the gate electrode (16).

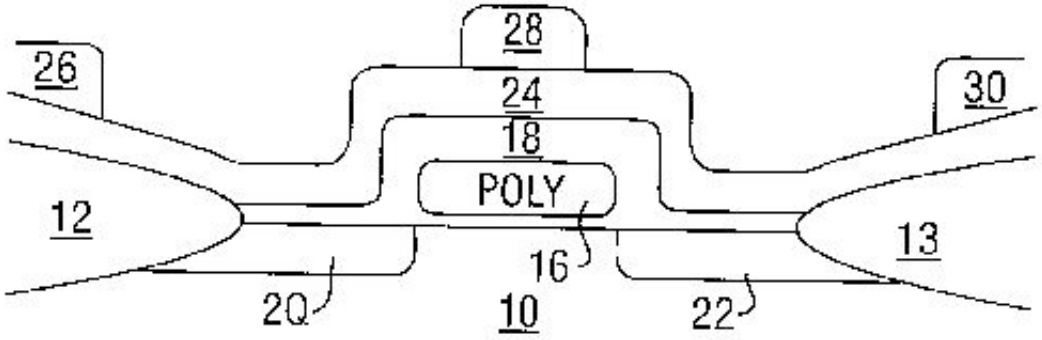

FIG. 2

There are a few inconsistencies between the specification and the claims of the "3 patent that bear noting. The specification purports to teach that, prior to the implantation stage, an *optional* anisotropic etch can be used to shape the differentially thermally grown oxide layer. For example, the specification states that an anisotropic etch can be used to thin or remove the layer of oxide over the substrate in order to increase the penetration of the implanted impurities. In addition, the specification suggests that an anisotropic etch can be used to thin the oxide on the sides of the gate electrode to create a smaller gap between the edges of the source/drain regions and the gate electrode. However, the claims all *require* that an anisotropic etch be performed before the implantation stage. Thus, to the extent that the specification teaches a process without anisotropic etching, that process would appear to fall outside the scope of the patent claims.

The specification also purports to teach "Alternative Techniques" to the preferred embodiment that do not involve differential growth of the oxide layer over the gate electrode and substrate. For example, these alternative techniques involve depositing nitride or silicon dioxide instead of growing an oxide. However, each of the claims of the "3 patent requires *growth* of a dielectric layer, and each requires that growth to be *differential*. Moreover, independent claims 1, 10, and 15 require the dielectric to be oxide. Thus, because these alternative techniques do not involve differential growth of a dielectric layer, this portion of the specification does not appear relevant to the claims as issued.

C. *Intel's Accused Processes*

TENA asserts that a number of Intel processes infringe the "3 patent, including Intel processes P652 and P852 (revs. 9 and 10). Intel argues that the P652 and P852 (revs. 9 and 10) processes do not infringe the "3 patent because these processes do not involve doping the gate electrode prior to differentially growing a dielectric layer over the MOS transistor, as is required by the patent. TENA denies that the "3 patent requires the manufacturer to dope the gate electrode prior to the differential growth step. Alternatively, TENA asserts that a genuine issue of material fact exists as to whether Intel does in fact dope the gate electrode prior to the differential growth step of the P652 and P852 (revs. 9 and 10) processes.

II. *DISCUSSION*

A. *What is the Standard for Summary Judgment?*

Summary judgment is appropriate when the evidence admissible at trial fails to demonstrate a genuine issue of material fact and when the moving party is entitled to judgment as a matter of law. *See, e.g.,* Brewer v. Quaker State Oil Refining Corporation, 72 F.3d 326, 329 (3d Cir.1995). In this case, Intel must show that TENA has presented insufficient evidence to carry its burden of persuasion at trial that Intel's processes infringe the "3 patent. Id. If Intel meets this burden, TENA must create a genuine issue of material fact such that a reasonable jury could return a verdict in its favor. Id. at 330 (citing Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 248, 106 S.Ct. 2505, 2510, 91 L.Ed.2d 202 (1986)).

[1] To determine whether Intel is entitled to a judgment as a matter of law that its processes do not infringe the "3 patent, the court must perform a two-step process. The court first must construe the claims of the patent. Texas Instruments, Inc. v. United States International Trade Commission, 988 F.2d 1165, 1171 (Fed.Cir.1993). The court then must compare the properly construed claims of the patent to the accused processes to determine if all of the limitations in the claims are present in these accused processes. Johnston v. IVAC Corporation, 885 F.2d 1574, 1577 (Fed.Cir.1989).

[2] [3] The construction of patent claims is a matter for the court. Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). In construing the words and phrases in a claim, the court should give those words and phrases their ordinary meaning, unless the specification clearly indicates that the inventor intended a different meaning. Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388 (Fed.Cir.1992). The court may also consider other words in the claim, other claims in the patent, the specification, the prosecution history, and expert testimony and other evidence outside of the patent. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979-81 (Fed.Cir.1995); Elf Atochem v. Libbey-Owens-Ford Co., 894 F.Supp. 844, 859 (D.Del.1995).

B. ***What are the Disputed Issues of Claim Construction?***

Intel presents one general claim construction question with respect to all of the claims of the "3 patent: Must the gate electrode be doped prior to differentially thermally growing the dielectric over the gate electrode, or can the gate electrode be doped during a later step of the process? Intel argues that the plain language of independent claims 1, 6, and 15 requires the manufacturer to dope the gate electrode prior to the differential thermal growth step. Furthermore, Intel argues that the specification and the prosecution history demonstrate the importance of doping for differential growth. TENA argues that differential growth can occur without doping, and that the claims allow for doping to occur at any time during the fabrication of an MOS transistor. Moreover, TENA argues that the specification and the prosecution history teach that doping may occur at any time and that the differential growth required by the patent does not require prior doping.

Examining independent claim 1 in light of Intel's general claim construction question, the court must construe the meaning of the phrases "forming a *doped* gate electrode ...; *then*" in step (a), and " *differentially* thermally *growing* an oxide ... whereby a *relatively thicker* layer of oxide is developed on the top and sides of the gate electrode and a *relatively thinner* layer of oxide is developed on the intended source and drain regions of the substrate" in step (b) (emphasis added).

Examining independent claim 6 in light of Intel's general question, the court must construe the meaning of the phrases "forming a *doped* polysilicon gate electrode" in step (a), and " *growing* a dielectric layer over the gate electrode by a process controlled to develop a *high differential of dielectric thickness* such that the dielectric is *relatively thick* over the top and sides of the gate electrode and *relatively thinner* over the intended source/drain regions" in step (b) (emphasis added).

Examining independent claim 15 in light of Intel's general question, the court must construe the meaning of the phrases "forming a *doped* gate electrode ...; *then*" in step (a), and " *establishing* an isolating oxide on the top and sides of the gate electrode and over the substrate adjacent the gate electrode such that the oxide on the top and sides of the gate electrode is *relatively thick compared to the oxide over the substrate,* including oxidizing in a steam atmosphere at a temperature which promotes *high differential rates of growth* of oxide as between the *doped* poly gate electrode and the substrate" in step (b) (emphasis added).

C. *What Does the Plain Language of the Claims Suggest?*

[4] The sequential order and language of claims 1, 6, and 15 suggests that doping must occur prior to the differential dielectric growth step. Step (a) in each claim recites a "doped" gate electrode, whereas step (b) in each claim recites differential dielectric growth. The ordering of the steps in this manner by itself implies a sequence. In addition, claims 1 and 15 both recite step (a) "then" step (b). The use of the word "then" further implies a sequence requiring doping first and then differential dielectric growth. Finally, step (b) of claim 15 includes steam oxidation that "promotes high differential rates of growth of oxide between the *doped* poly gate electrode and the substrate" (emphasis added). By referring back to structure formed in step (a), the use of the word "doped" in step (b) further implies that the doping must occur prior to the differential dielectric growth step. *See* Loral Fairchild Corp. v. Victor Co. of Japan, Ltd., 906 F.Supp. 798, 805 (E.D.N.Y.1995) (stating that the ordering of the steps of a process patent in combination with language in subsequent steps referring back to structure formed in previous steps strongly suggests that the steps must proceed in chronological order).

The use of the term "differential" in step (b) of claims 1, 6, and 15 also suggests that doping must occur prior to the dielectric growth step. It is known in the art that doping the gate electrode prior to growing a dielectric layer over the entire MOS transistor will cause the oxide to grow much faster over the doped gate electrode as compared to over the undoped substrate. For example, claim 10 itself recites that the gate electrode "is doped to promote a high rate of differential thermal oxidation." Thus, an individual skilled in the art of making MOS transistors might consider the recitation of a "doped" gate electrode in step (a) as a necessary requirement for producing the required differential thermal growth of step (b). Between the sequential ordering of the steps and the scientific logic of the sequence from the perspective of those skilled in the art of making MOS transistors, the common sense reading of claims 1, 6, and 15 would require the doping of the gate electrode to occur prior to differential dielectric growth.

Finally, with respect to claim 6, steps (f) and (g) recite that the dielectric layer grown during step (b) must remain on top of the gate electrode even after the contact points have been formed. This requirement suggests that it would be practically impossible to dope the gate electrode after the dielectric growth step. The declaration of Dr. Chung, Intel's expert, states that "one skilled in the art [of making MOS transistors] would not believe that it would be practical to dope the polysilicon after the thick dielectric is formed on the polysilicon because that thick dielectric would make it difficult to access the polysilicon to dope it." Therefore, this additional limitation of claim 6 confirms as a practical matter that doping must occur prior to the dielectric growth step.

D. *What are TENA's Arguments In Opposition to This Construction Based on the Plain Language of the Claims?*

TENA makes five arguments in opposition to this plain meaning construction of the claims. First, TENA argues that the patent does not teach, and those skilled in the art were unaware at the time the "3 patent

issued, that doping must precede dielectric growth. Second, TENA argues that because the explicit language of claim 10 requires doping prior to differential growth, and because the same language is missing from claims 1, 6, and 15, that the doctrine of claim differentiation prevents the court from construing such a limitation into claims 1, 6, and 15. Third, TENA argues that the word "then" was added to the claims before the word "doped" and thus does not relate to the sequence of when the gate electrode must be doped. Fourth, TENA argues that dependent claims 16 and 17 do not require doping prior to differential growth, and thus the court cannot construe independent claim 15 to have such a limitation. Fifth, TENA argues that the prior art does not require prior doping of the gate electrode in order to render the "3 patent nonobvious. As set out below, these arguments are unavailing in light of the plain claim language, the specification, and the prosecution history.

1. *Does the patent teach that doping must precede dielectric growth?*

TENA argues that those skilled in the art would have been unaware that doping must precede dielectric growth in the "3 patent. First, TENA asserts that the patent does not teach that doping promotes differential growth. Rather, TENA argues that those skilled in the art would understand doping only to refer to improving the electrical conductivity of the gate electrode, which suggests that doping can occur at any time during the process. Second, TENA argues that the "Alternative Techniques" section of the specification describes a version of the patented process that dopes the gate electrode after dielectric growth. Third, TENA argues that the final paragraph of the specification, which states that "the sequence in which some steps are practiced may be altered to suit a particular application or processing environment," indicates that doping need not occur prior to the differential thermal growth step.

Contrary to TENA's first assertion, claim 10, at column 10, lines 7-9, and the specification, at column 3, lines 30-33, specifically state that doping increases differential dielectric growth. Therefore, even if those skilled in the art were not aware prior to the issuance of the patent that doping promotes differential growth, the patent clearly teaches that effect. In addition, as set out above in the description of the preferred embodiment, the "Alternative Techniques" do not involve differential dielectric growth and thus do not appear relevant to the patent claims as issued. According to Dr. Chung's declaration,the initial claims in the "3 patent did not require differential growth and thus supported this section of the specification. However, when Mr. Manzo, the prosecuting attorney for the "3 patent, added the differential growth limitation during the prosecution, these "Alternative Techniques" became irrelevant. Based on the prosecution history as set out below in the discussion of TENA's claim differentiation argument, Dr. Chung's characterization appears to be correct.

Even if these "Alternative Techniques" were relevant, however, the mere fact that doping *can* occur at any stage of the process in order to give the gate electrode its *electrical conductivity* does not answer the question of whether the patent claims nevertheless *require* doping prior to the growth of the dielectric to promote *differential growth*. TENA cannot use the "Alternative Techniques" section or the generic catch-all paragraph at the end of the specification to overcome specific limitations of the claims. *See* Unique Concepts, Inc. v. Brown, 939 F.2d 1558, 1562 (Fed.Cir.1991) (stating that a patentee cannot use the specification to avoid specific limitations of his claims and to interpret a claim contrary to its plain meaning).

2. *Does the doctrine of claim differentiation prevent the court from construing claims 1, 6, and 15 to require doping prior to dielectric growth?*

TENA admits that claim 10 requires doping prior to dielectric growth. However, TENA argues that the

language of claim 10 that requires this limitation, read in connection with the prosecution history, establishes that prior doping is required only for the differential growth of claim 10. Thus, under the doctrine of claim differentiation, the court cannot construe claims 1, 6, and 15 to require doping for differential growth. TENA's argument requires a detailed examination of the relevant prosecution history.

a. *A chronology of the relevant prosecution history*

1) *The language of the claims as filed*

When Manzo first filed the application that resulted in the "3 patent, the patent had only two independent claims. These two claims ultimately issued as claims 1 and 6 of the "3 patent. As initially filed, claim 1 stated in relevant part:

....

(a) forming a gate electrode insulated from the substrate;

(b) forming an implant mask of a controlled width on the sides of the gate electrode;

....

As initially filed, claim 6 stated in relevant part:

....

(b) defining a polysilicon gate electrode over the gate insulator between the intended source/drain regions;

(c) establishing a dielectric layer over the gate electrode and the gate insulator such that the dielectric is relatively thick at least over the sides of the gate electrode and relatively thinner over the intended source/drain regions

....

Neither claim 1 nor claim 6 contained the words "doped" or "then" or the phrases "differentially thermally growing" or "differential growth." However, claim 6 contained language suggesting that a differential must exist between the dielectric over the sides of the gate electrode, where it must be "relatively thick," and over the intended source/drain regions, where it must be "relatively thinner."

2) *The first rejection and amendment*

The Patent and Trademark Office ("PTO") examiner rejected TENA's claims as obvious in light of the combination of U.S. Patent No. 4,182,023 issued to Cohen *et al*. (the "Cohen patent") and U.S. Patent No. 4,234,362 issued to Riseman (the "Riseman patent"). The examiner observed that Cohen discloses a layer of oxide overhanging the gate electrode that acts as a shield to prevent the source/drain regions from being implanted next to the gate electrode. Therefore, a subsequent heat driving step would laterally diffuse the edges of the source/drain regions until they were in substantial alignment with the edges of the gate electrode.

In response to this rejection, Manzo added the word "then" after step (a) of claim 1. To explain this change, Manzo stated that the Cohen patent requires the implant mask to be formed before or simultaneously with the gate electrode. Conversely, the invention of the "3 patent forms the gate electrode and "then" forms the implant mask. Although Manzo did not add the word "then" to claim 6, it appears from his argument that the sequence of forming the gate electrode prior to forming the implant mask was important in distinguishing the Cohen patent.

3) *Subsequent rejections and amendments*

Manzo filed additional amendments to the two independent claims in response to two subsequent rejections that are not relevant here. However, Manzo did file two relevant new independent claims, which ultimately issued as claims 10 and 15 of the "3 patent. As initially filed, claim 10 stated in relevant part:

....

(a) forming a defined gate insulated from and over a substrate; then

(b) establishing an isolating oxide layer of controlled dimensions by a *differential thermal growth* process such that the oxide layer covers the top and sides of the gate and regions in the substrate where the source and drain will be formed, the oxide being *thicker* on the top and sides of the gate than above the prospective source and drain; then

.... (emphasis added)

As initially filed, claim 15 stated in relevant part:

....

[(a)] forming a gate electrode insulated from the substrate; then

[(b)] establishing a dielectric on the top and sides of the gate electrode and over the substrate adjacent to the gate electrode such that the dielectric on the top and sides of the gate electrode is *relatively thick* compared to the dielectric over the substrate;

.... (emphasis added)

Thus, claim 10 was the first independent claim specifically to recite "differential thermal growth." Claims 6 and 15 contained language suggesting some differential between the dielectric layer over the gate electrode and the layer over the substrate, albeit not necessarily from thermal growth.

Manzo also amended some of the dependent claims in ways that are relevant to the present discussion. In particular, he added differential thermal growth to some of the dependent claims to establish a more narrow basis for patentability. In addition, he further added anisotropic etching to some of these dependent claims. Manzo argued that, at a minimum, the prior art never suggested using differential thermal growth in combination with anisotropic etching to make a zero overlap MOS transistor.

4) *Final rejection*

The examiner issued a final rejection of all of the claims in spite of these amendments. Specifically, the examiner stated that the claims were obvious in light of the combination of the Cohen patent and U.S. Patent No. 4,139,402 issued to Steinmaier *et al*. (the "Steinmaier patent"):

Steinmaier et al[.] discloses forming an insulated polysilicon gate on a substrate, growing a thermal oxide over the gate and substrate, implanting source and drain regions on either side of the gate through the thin oxide over the substrate, heat driving the source and drain, and forming contacts. The thermally grown oxide is inherently thicker on the top and sides of the polysilicon gate than on the silicon substrate.... It would be obvious to routinely optimize the process of Steinmaier et al[.] to obtain the advantages of the aligned, nonoverlapping gate structure of Cohen et al.

Thus, the examiner determined that even the dependent claims, some of which contained both differential thermal growth and anisotropic etching, were obvious in light of the prior art.

5) *Manzo's "First Proposed Amendment"*

In his "First Proposed Amendment After Final Rejection," Manzo made substantial changes to the patent claims. He amended claim 1 to state in relevant part:

....

(a) forming a *doped* polysilicon gate electrode upon but insultated [sic] from a monocrystalline silicon substrate; then

(b) *differentially thermally growing* an implant mask of oxide of a controlled thickness on both the sides and on the top of the gate electrode *including controlling ambient conditions* to promote a high rate of oxidation on the top and sides of the doped polysilicon gate compared to the silicon substrate, whereby a *relatively thicker* layer of oxide is developed on the top and sides of the gate and a *relatively thinner* layer of oxide is developed on the intended source and drain regions of the substrate; then.... (emphasis added)

Manzo amended claim 6 to state in relevant part:

....

(b) forming a *heavily doped* polysilicon gate electrode over the gate insulator ...; then

(c) establishing a dielectric layer over the gate electrode ... by a process controlled to develop a *high differential of dielectric thickness* as between the gate and other areas such that the dielectric is relatively thick over the top and sides of the gate electrode and relatively thinner over the intended source/drain regions;

.... (emphasis added)

Manzo amended claim 10 to state in relevant part:

....

(a) forming a defined gate insulated from and over a substrate, said gate being *doped to promote a high rate of differential thermal oxidation,* said substrate being monocrystalline silicon; then

(b) establishing an isolating oxide layer on the top and sides of said gate by *thermal oxidation under ambient conditions* controlled such that the oxide layer covers the top and sides of the gate and regions in the substrate where the source and drain will be formed, the oxide growing *substantially thicker* on the top and sides of the gate than above the prospective source and drain; then

.... (emphasis added)

Finally, Manzo amended claim 15 to state in relevant part:

....

[(a)] forming a gate electrode insulated from the substrate, said *gate* being polysilicon *doped to a sheet resistance of about 20 ohms per square,* said substrate being monocrystalline silicon; then

[(b)] establishing a dielectric on the top and sides of the gate electrode and over the substrate adjacent to the gate electrode such that the dielectric on the top and sides of the gate electrode is *relatively thick* compared to the dielectric over the substrate, said establishing step including *oxidizing in a steam atmosphere* at a temperature which promotes *high differential rates of growth* as between the *doped* poly gate and the substrate;

.... (emphasis added)

When Manzo submitted these amendments, he explained in detail the reasons for the changes. In particular, he focused on the examiner's conclusion as a part of his final rejection that the Steinmaier patent inherently disclosed differential growth. Manzo argued that although some differential growth does occur between a gate electrode constructed of one material and a substrate constructed of another, as in the Steinmaier patent, this differential is very small. He argued that differential dielectric growth is more dependent upon the doping of the elements and the ambient conditions, which include the temperature and water content of the atmosphere during the dielectric growth step.

In support of his arguments, Manzo submitted an article by T.I. Kamins entitled "Oxidation of Phosphorous-Doped Low Pressure and Atmospheric Pressure CVB Polycrystalline-Silicon Films," in Volume 126 of the *Journal of the Electrochemical Society: Solid State Science and Technology* (May 1979) (the "Kamins article"). Manzo stated that the Kamins article demonstrates that when an undoped polysilicon gate electrode on a monocrystalline substrate is placed in a dry oxygen gas atmosphere over a temperature range of 950 (deg.) C to 1150 (deg.)C, there will be 7% to 9% greater thickness of oxide on the gate electrode. However, based on the Kamins article, Manzo stated that when the ambient conditions are changed to include a steam atmosphere, a differential of 30-35% results. Moreover, Manzo stated that if the gate electrode is doped first, the Kamins article demonstrates that a differential of 300% results.

Manzo contrasted the Steinmaier patent by observing that it recited dielectric layers of "substantially equal thickness" because it involved dry oxidation without doping. He emphasized that in the Steinmaier patent, "polysilicon gate 14 is *not doped* at the time of oxidation" (emphasis in original). He then described the preferred embodiment of the "3 patent, stating that doping of the gate electrode to a sheet resistance of 20

ohms per square is " *very substantial doping*" (emphasis in original). Manzo further stated:

It will be appreciated that the poly[silicon gate electrode] oxide grows about 300% faster that the monocrystalline silicon [substrate] oxide. This accords with the teachings of Kamins in Table I which shows that at a temperature of 850 (deg.)[C], the differential between highly doped polysilicon and slightly doped crystal silicon in a steam atmosphere is 327% . This is *an enormous difference in kind* between the dry oxidation of an undoped polysilicon gate on an exposed single crystal silicon substrate, where the differential is [7%]. (emphasis in original)

Thus, Manzo distinguished the inherent differential growth between an undoped polysilicon gate electrode and a monocrystalline silicon substrate, as shown by the Kamins article and the Steinmaier patent, from the differential growth of the "3 patent.

The changes to the claims reflect Manzo's arguments that doping and ambient conditions create greater differential growth than recognized by the Steinmaier patent. To claim 1 he added "doped" and "controlling ambient conditions to promote a high rate of oxidation on the top and sides of the doped polysilicon gate compared to the silicon substrate, whereby a relatively thicker layer of oxide is developed on the top and sides of the gate and a relatively thinner layer of oxide is developed on the intended source and drain regions of the substrate." To claim 6 he added "heavily doped" and "a process controlled to develop a high differential of dielectric thickness as between the gate and other areas." To claim 10 he added "doped to promote a high rate of differential thermal oxidation" and "thermal oxidation under ambient conditions controlled such that ... the oxide grow[s] substantially thicker on the top and sides of the gate than above the prospective source and drain." Finally, to claim 15 he added "doped to a sheet resistance of about 20 ohms per square" and "establishing a dielectric ..., said establishing step including oxidizing in a steam atmosphere at a temperature which promotes high differential rates of growth as between the doped poly gate and the substrate."

The examiner stated in response to these amendments that he would not consider new limitations to the claims after final rejection. Instead, he stated that Manzo would have to file a continuation application. Manzo subsequently filed a request for a File Wrapper Continuing Application (the "FWC request").

6) *The FWC request*

Manzo focused almost exclusively on the Steinmaier patent in his FWC request. He strenuously attempted to distinguish the Steinmaier patent from the processes claimed in the "3 patent based on the differential growth resulting from the doping of the gate electrode:

There is absolutely no mention that oxidation growth in the Steinmaier patent is differential in nature.... [T]here is not even a clue in the Steinmaier patent that if the poly [gate electrode] layer were doped prior to the formation of the oxide layer 21, there would be an even thicker formation of oxide on the top and sides of the gate.... Applicants submit *that there is nothing whatsoever in Steinmaier et al. alone which suggests that there is an advantage in doping the poly layer*. (emphasis in original)

Manzo further argued that combining the Steinmaier and Cohen patents still failed to teach the advantage of doping the gate electrode "to promote a high rate of oxidation."

Subsequent to the submission of the FWC request, the examiner interviewed Manzo to discuss claims 1, 6,

and 15 in light of the Cohen and Steinmaier patents. The examiner stated the following in his "Examiner Interview Summary Record" ("EISR"): "Mr. Manzo to submit preliminary amendment to place case in condition for allowance. Anisotropic etching limitation to be added to claims 1, [6, and 15]." At this point, independent claim 10 already had an anisotropic etching step. In response to the EISR, Manzo submitted a voluntary amendment.

7) *The voluntary amendment*

As part of Manzo's voluntary amendment, he added an anisotropic etching step after the differential dielectric growth step of claims 1, 6, and 15. He also removed some relevant language from each of the claims. In claim 1 Manzo removed "controlling ambient conditions to promote a high rate of oxidation on the top and sides of the doped polysilicon gate compared to the silicon substrate." In claim 6 he replaced "heavily doped" with "doped" and "establishing a dielectric layer" with "growing a dielectric layer." Finally, in claim 15 he replaced "said gate being polysilicon doped to a sheet resistance of about 20 ohms per square" with "doped gate electrode."

Manzo explained that he amended the claims to include anisotropic etching to overcome a rejection based on a U.S. Patent No. 4,400,866 issued to Yeh *et al*. (the "Yeh patent"). Apparently, the examiner cited the Yeh patent "to show differential oxidation for providing a gap for a source/drain implant." Manzo did not explain why he removed the additional language from the claims. He merely stated that the independent claims include features of a doped gate and differential dielectric growth.

b. *Is TENA's claim differentiation argument valid?*

TENA now asserts that when the examiner issued his EISR requiring the additional limitation of an anisotropic etching step, he was indicating to Manzo that the patent claims did not require "substantial" differential growth as recited by claim 10. Therefore, TENA asserts that Manzo amended claims 1, 6, and 15 to provide for lesser levels of differential growth. For example, claim 1 only requires a "relatively thicker layer of oxide" over the gate electrode, and claims 6 and 15 require that the oxide layer is "relatively thick" over the gate electrode. However, Manzo left the language in claim 10 that requires doping of the gate electrode "to promote a high rate of differential thermal oxidation" resulting in a "substantially thicker" layer of oxide over the gate electrode. Based on these assertions, TENA argues that the doctrine of claim differentiation prevents the court from construing claims 1, 6 and 15 to require prior doping to promote "substantial" differential dielectric growth.

As a threshold matter, TENA's argument contains a number of factual weaknesses. The EISR is ambiguous and does not support clearly TENA's assertion that the examiner did not think "substantial" differential growth was important to allowing the claims. To the contrary, the court could as easily interpret the EISR as supporting the notion that "substantial" differential growth was a necessary but insufficient condition for allowance. In addition, Manzo's removal of some language from the claims does not indicate clearly that doping was not important for differential growth. Manzo did not remove the word "doped" from the first step of claims 1, 6, and 15, nor did he remove the differential language from each of these claims. In particular, claims 6 and 15 still recite that "a high differential" of growth is required.

[5] Even assuming that TENA's assertions regarding the EISR and Manzo's amendments are factually correct, however, TENA's claim differentiation argument suffers from two fundamental errors. The doctrine of claim differentiation prohibits construing one claim to include a limitation expressed in another claim if that construction renders one of the claims "superfluous." Tandon Corporation v. United States International

Trade Commission, 831 F.2d 1017, 1023-24 (Fed.Cir.1987). The first error is that there are a number of differences between the independent claims beyond the level of differential growth that is required, such as the requirement of contact points, the use of dielectrics other than oxide, and so on. Thus, the court need not find a difference between the required levels of differential growth merely to prevent the claims from being "superfluous." *See id*.

Second, the court can construe the claims as providing for different levels of differential growth consistently with the notion that doping of the gate electrode must occur first. Differential growth depends both on the amount of doping and on the ambient conditions during the growth stage. Lighter doping of the gate electrode might suffice for claim 1 because that claim does not require a "high differential" of dielectric growth as do claims 6 and 15. Furthermore, claim 15 requires steam oxidation, which will further increase the differential rate of growth over that which results from merely doping the gate electrode. In other words, Manzo's amendments affected how much doping or differential growth was required by each of the claims, not whether doping must precede dielectric growth. In fact, Manzo's removal of the "ambient conditions" language from claim 1, rather than implying that "substantial" differential growth is not important, more logically underscores the importance of doping alone to create sufficient differential growth to overcome the examiner's rejections over the Steinmaier patent and the Kamins article.

3. ***What is the effect of adding the word "then" prior to the word "doped" in claims 1 and 15?***

TENA is correct that the word "then" was added to claims 1 and 15 before the word "doped." However, it is not at all clear that this fact alone would suggest that "then" does not apply to doping. As set out above, the plain language and sequential ordering of the claims in conjunction with the word "then" suggests that doping is required prior to differential dielectric growth. Moreover, when Manzo added the doping requirement in step (a) of each claim, he continually argued to the examiner that the doping was necessary to create sufficient differential growth to overcome the Steinmaier patent. At that point, the word "then" took on greater significance than requiring that the gate electrode be formed prior to the formation of the implant mask. The word "then" took on its natural meaning that each part of the preceding step had to be completed prior to the following step. This includes the requirement that the gate electrode be "doped" prior to differential dielectric growth.

4. ***Do claims 16 and 17 prevent the court from construing claim 15 to require doping prior to differential growth?***

TENA argues that dependent claims 16 and 17 specifically allow for doping during the implantation of the source/drain regions. Thus, TENA argues that claims 16 and 17 recognize that doping need not occur prior to the differential growth step. TENA then argues that the court cannot construe claim 15, from which claims 16 and 17 depend, more narrowly than the required scope of claims 16 and 17. In other words, the court cannot construe claim 15 to require doping of the gate electrode prior to the differential thermal growth stage when claims 16 and 17 do not require this sequence.

Assuming for the sake of argument that TENA is correct in its assertion that claims 16 and 17 allow for doping during the implantation step, it does not follow necessarily that claims 16 and 17 recognize that doping need not occur prior to the differential growth step. An alternate reading of claims 16 and 17 suggests that the gate electrode can be doped prior to *and* after the differential growth stage. This reading is consistent with independent claim 15's requirement that doping must occur prior to differential growth. TENA argues, again under the banner of claim differentiation, that this reading would render claims 16 and 17 superfluous. However, Dr. Chung's declaration states that a second doping can produce improved

electrical conductivity. Thus, reciting the possibility of a second doping after the differential dielectric growth step does not appear to render claims 16 and 17 "superfluous."

TENA's reading of claims 16 and 17 would require the court to remove the specific limitation in independent claim 15 that doping of the gate electrode must occur prior to differential thermal growth. The court cannot use a potentially broad reading of a dependent claim to ignore a specific limitation of the independent claim from which it depends, particularly when a logical alternative reading of the dependent claim exists.

5. *Does it matter if the prior art does not require doping of the gate electrode prior to differential dielectric growth?*

[6] TENA argues that no prior art requires doping of the gate electrode prior to differential dielectric growth. Even if that were true, TENA cannot now eliminate a specific claim limitation that Manzo added to overcome a rejection by the PTO. *See* Parks v. Fine, 773 F.2d 1577, 1579 (Fed.Cir.1985) (stating that the insertion of a limitation to overcome an examiner's rejection is strong evidence of materiality); Kinzenbaw v. Deere & Co., 741 F.2d 383, 389 (Fed.Cir.1984). Manzo ardently argued to the examiner that the Steinmaier patent did not teach doping the gate electrode to achieve differential growth. Moreover, Manzo never withdrew the word "doped" from step (a) of each of the claims even after he added the anisotropic etching step, and he never commented to the examiner that the sequential order of prior doping was no longer material to allowance of the claims. Given the plain meaning of the claim language, the teachings of the specification, and Manzo's arguments before the PTO, the court can only conclude that all of the claims of the "3 patent require doping of the gate electrode prior to the differential dielectric growth step.

E. *Do Intel's P652 and P852 (revs. 9 and 10) Processes Infringe* the "3 Patent *When Properly Construed?*

[7] Having construed the relevant portions of the claims 1, 6, and 15, to require doping of the gate electrode prior to differentially growing a dielectric implant mask, the court must ascertain whether Intel's P652 and P852 (revs. 9 and 10) processes fail to follow this sequence and thus do not infringe the "3 patent. Intel asserts that these processes do not dope prior to a differential dielectric growth step. In response, TENA asserts that material facts are in dispute precluding summary judgment. However, TENA's "disputed material facts" consist of disputed constructions of the patent terms and different interpretations of the effect of the prosecution history, which are insufficient to preclude summary judgment. *See* Becton Dickinson and Co. v. C.R. Bard, Inc., 922 F.2d 792, 797 (Fed.Cir.1990).

TENA's expert Dr. Fair appears to admit in his declaration that Intel's P652 and P852 (revs. 9 and 10) processes do not dope the gate electrode prior to differentially growing a dielectric layer. TENA cites no other evidence in support of its argument that a genuine issue of material fact exists as to whether Intel dopes the gate electrode first. Thus, the court must conclude that no material facts are in dispute and that Intel is entitled to judgment as a matter of law that its P652 and P852 (revs. 9 and 10) do not infringe claims 1, 6, and 15 of the "3 patent.

[8] TENA contends that even if the claims of the "3 patent require doping during step (a), there are "insubstantial differences between the claimed and accused products or processes." Hilton Davis Chemical Co. v. Warner-Jenkinson Co., 62 F.3d 1512, 1521-22 (Fed.Cir.1995) (*en banc*). Thus, TENA argues that a question of fact exists as to whether Intel's processes infringe the claims of the "3 patent under the doctrine of equivalents. However, when an accused process does not perform a required step of the claimed process, there is no infringement either literally or under the doctrine of equivalents. *See* London v. Carson Pirie

Scott & Co., 946 F.2d 1534, 1539, 1539 (Fed.Cir.1991). Intel's relevant processes do not form a "doped gate electrode" as the first step. Thus, these processes do not infringe under the doctrine of equivalents.

[9] [10] Prosecution history estoppel also bars TENA's doctrine of equivalents argument. Prosecution history estoppel prevents TENA from using the doctrine of equivalents to resurrect material previously surrendered during the prosecution of the "3 patent. Texas Instruments, 988 F.2d at 1173. Prosecution history estoppel is a question of law for the court. Hoganas AB v. Dresser Industries, Inc., 9 F.3d 948, 952 (Fed.Cir.1993). Here, Manzo attempted to overcome multiple rejections based on the Steinmaier patent by emphasizing the importance of prior doping of the gate electrode to promote differential growth. Furthermore, he amended all of the claims to include doping in step (a) and differential growth in step (b). These actions by Manzo are sufficient to estop TENA from arguing now that the sequence of doping and then differentially growing a dielectric layer is not a material limitation of the claims of the "3 patent.

III. ***CONCLUSION***

All of the claims of the "3 patent require doping of the gate electrode prior to differentially growing a dielectric layer over the MOS transistor. It is undisputed that Intel's P652 and P852 (revs. 9 and 10) do not dope the gate electrode prior to a differential dielectric growth step. Thus, Intel's processes do not infringe the "3 patent literally or under the doctrine of equivalents, and Intel is entitled to judgment as a matter of law.

The court will issue an Order in accordance with this Opinion.

D.Del.,1996.
Thorn EMI North America, Inc. v. Intel Corp.

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