United States District Court,
S.D. California.

QUALCOMM INCORPORATED,
Plaintiff.
v.
BROADCOM CORPORATION,
Defendants.
Broadcom Corporation,
Counter-Claimant.
v.
Qualcomm Incorporated,
Counter-Defendant.

Civil No. 05CV1392-B(BLM)

June 20, 2006.

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CLAIM CONSTRUCTION ORDER FOR UNITED STATES PATENT NUMBER 6,075,807

RUDI M. BREWSTER**, Senior Judge.**

Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), on June 5-8, 2006, the Court conducted a Markman hearing concerning the above-titled patent infringement action regarding construction of the disputed claim terms for U.S. Patent Number 6,075,807 ("the '807 patent"). Plaintiff Qualcomm, Inc. was represented by the law firm of Heller Ehrman LLP, and Defendant Broadcom Corp. was represented by the law firm of McAndrews, Held & Malloy, Ltd.

At the Markman hearing, the Court, with the assistance of the parties, analyzed the claim terms in order to prepare jury instructions interpreting the pertinent claims at issue in the '807 patent. Additionally, the Court prepared a case glossary for terms found in the claims and specification for the '807 patent considered to be technical in nature which a jury of laypersons might not understand clearly without a specific definition.

After careful consideration of the parties' arguments and the applicable statutes and case law, the Court **HEREBY CONSTRUES** the claims in dispute for the '807 patent and **ISSUES** the relevant jury instructions as written in Exhibit A, attached hereto. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED.

EXHIBIT A FN1

UNITED STATES PATENT NUMBER 6.075.807-CLAIM CHART

VERBATIM CLAIM LANGUAGE	**COURT'S CONSTRUCTION**
Claim 1	**Claim 1**
1. A digital matched filter for a CDMA radio system comprises:	1. A digital matched filter for a CDMA radio system ***comprises*** [*includes but is not limited to*]:
a digital delay line having a plurality of successive delay stages adapted to receive a multiple bit digital signal and propagate said digital signal therethrough at a fixed rate;	a ***digital delay line having a plurality of successive delay stages adapted to receive a multiple bit digital signal and propagate said digital signal therethrough at a fixed rate*** [*a device that moves a multiple bit digital signal through successive storage locations at a fixed rate. The multiple bit digital signal is delayed by being held in each storage location*];
a correlator coupled to said digital delay line to correlate said digital signal to a predefined spreading code to provide a plurality of signals indicating correspondence between individual bits of said digital signal and respective chips of said spreading code;	a ***correlator*** [*device which is capable of comparing two signals to determine whether they agree or disagree*] ***coupled*** [*operatively connected*] to said ***digital delay line*** to ***correlate*** [*compare two signals to determine whether they agree or disagree*] said digital signal to a predefined ***spreading code*** [*a predetermined length sequence of chips that is used to modulate or 'spread' the signal before it is sent and that is used to demodulate or despread the signal after it is received*] to provide a ***plurality*** [*two or more*] of signals indicating correspondence between individual ***bits*** [*characters used to represent one of two digits in a system having two possible states, e.g., high or low, on or off, one or zero, +1 or -1, true or false, etc.*] of said digital signal and respective ***chips of said spreading code*** [*the signals corresponding to the individual components of the spreading code*];
a summing device coupled to said	a summing device ***coupled*** to said ***correlator*** to combine said ***plurality*** of

correlator to combine said plurality of signals into a summed signal representing a degree of correlation of said digital signal to said spreading code; and	signals into a summed signal representing a degree of ***correlation*** [*agreement or disagreement*] of said digital signal to said spreading code; and
a window control unit operatively coupled to said summing device to enable operation of at least one of said correlator and said summing device only during discrete time periods of said summed signal having a high degree of correlation of said digital signal to said spreading code, and disable operation of at least one of said correlator and said summing device between said successive ones of said discrete time periods.	a window control unit operatively coupled to said summing device to enable operation of at least one of said correlator and said summing device only during ***discrete time periods*** [*windows of time*] of said summed signal having a high degree of correlation of said digital signal to said spreading code, and disable operation or at least one of said correlator and said summing device between said successive ones of said discrete time periods.
Claim 2	**Claim 2**
2. The digital matched filter of claim 1, wherein said correlator further comprises a plurality of logic gates each having a first input coupled to a corresponding one of said stages of said digital delay line and a second input coupled to a corresponding bit of said spreading code.	2. The digital matched filter of claim 1, wherein said ***correlator*** further ***comprises*** a ***plurality*** of ***logic gates*** [*basic electrical building blocks where the state of a logic gate's output is determined by the states of its inputs*] each having a first input ***coupled*** to a corresponding one of said stages of said ***digital delay line*** and a second input ***coupled*** to a corresponding ***bit*** of said ***spreading code.***
Claim 3	**Claim 3**
3. The digital matched filter of claim 2, wherein said logic gates further comprise exclusive-OR logic gates.	3. The digital matched filter of claim 2, wherein said ***logic gates*** further ***comprise exclusive-OR logic gates*** [*logic gates whose outputs are true if either of one of its respective inputs, but not both inputs, is true*].
Claim 4	**Claim 4**
4. The digital matched filter of claim 2, wherein said logic gates further comprise CMOS logic gates.	4. The digital matched filter of claim 2, wherein said ***logic gates*** further **comprise CMOS** [*a particular class of semiconductor*] ***logic gates.***
Claim 5	**Claim 5**
5. The digital matched filter of claim 1, further comprising a system clock providing a clock signal for said correlator and said summing device, said window control unit providing an	5. The digital matched filter of claim 1, further ***comprising*** [*including but not limited to*] a system clock providing a clock signal for said ***correlator*** and said summing device, said window control unit providing an enabling signal to enable said clock signal to reach said ***correlator*** and said summing device.

enabling signal to enable said clock signal to reach said correlator and said summing device.	
Claim 6	**Claim 6**
6. The digital matched filter of claim 5, further comprising a bit synchronization unit coupled to said window control unit to receive said correlation signal and derive a data signal therefrom, and an AND gate adapted to receive said clock signal and said enabling signal, said AND gate further having an output coupled to clock inputs of said correlator and said bit synchronization unit.	6. The digital matched filter of claim 5, further ***comprising*** a ***bit synchronization unit*** [*a circuit that synchronizes the timing of the digital matched filter to the received. signal*] ***coupled*** to said window control unit to receive said ***correlation signal*** [*a signal indicating* ***correlation***] and derive a data signal therefrom, and an ***AND gate*** [*a* ***logic gate*** *whose output is true if and only if all of its inputs are true*] adapted to receive said clock signal and said enabling signal, said ***AND gate*** further having an output ***coupled*** to clock inputs of said ***correlator*** and said ***bit synchronization unit.***
Claim 8	**Claim 8**
8. A digital matched filter for a CDMA radio system comprises:	8. A digital matched filter for a CDMA radio system ***comprises:***
a digital delay line having a plurality of successive delay stages adapted to receive a multiple bit digital signal and propagate said digital signal therethrough at a fixed rate;	a ***digital delay line having a plurality of successive delay stages adapted to receive a multiple bit digital signal and propagate said digital signal therethrough at a fixed rate;***
a correlat[or] coupled to said digital delay line to correlate said digital signal to a predefined spreading code to provide a plurality of signals indicating correspondence between individual bits of said digital signal and respective chips of said spreading code;	a ***correlat[or] coupled*** to said ***digital delay line*** to ***correlate*** said digital signal to a predefined ***spreading code*** to provide a ***plurality*** of signals indicating correspondence between individual ***bits*** of said digital signal and respective ***chips of said spreading code;***
a summing device coupled to said correlator to combine said plurality of signals into a summed signal representing a degree of correlation of said digital signal to said spreading code;	a summing device ***coupled*** to said ***correlator*** to combine said ***plurality*** of signals into a summed signal representing a degree of ***correlation*** of said digital signal to said ***spreading code;***
a window control unit operatively coupled to said summing device to enable operation of at least one of said correlator and said	a window control unit operatively coupled to said summing device to enable operation of at least one of said correlator and said summing device only during ***discrete time periods*** of said summed signal having a high degree of correlation of said digital signal to said spreading code,

summing device only during discrete time periods of said summed signal having a high degree of correlation of said digital signal to said spreading code, and disable operation of at least one of said correlator and said summing device between said successive ones of said discrete time periods; and	and disable operation of at least one of said correlator and said summing device between said successive ones of said discrete time periods; and
bit synchronization unit coupled to said window control unit to receive said correlation signal and derive a data signal therefrom.	a ***bit synchronization unit*** coupled to said window control unit to receive said ***correlation signal*** and derive a data signal therefrom.
Claim 14	**Claim 14**
14. A method for reducing power consumption in a CDMA radio system, comprises:	14. A method for reducing power consumption in a CDMA radio system, ***comprises:***
propagating a received digital signal through a digital delay line having a plurality of successive delay stages;	***propagating a received digital signal through a digital delay line having a plurality of successive delay stages*** [*moving a digital signal through successive storage locations. The digital values are delayed by being held in each storage location*];
correlating said digital signal to a predefined spreading code to provide a correlation signal reflecting a degree of correlation of said digital signal to said spreading code;	***correlating*** said digital signal to a predefined ***spreading code*** to provide a ***correlation signal*** reflecting a degree of ***correlation*** of said digital signal to said ***spreading code:***
deriving a data signal and a clock signal from said correlation signal, said correlation signal comprising discrete time periods which correspond to correlation of said digital signal to said spreading code; and disabling performance of said correlating step between said discrete time periods.	deriving a data signal and a clock signal from said ***correlation signal,*** said ***correlation signal comprising discrete time periods*** which correspond to ***correlation*** of said digital signal to said ***spreading code:*** and disabling performance of said correlating step between said ***discrete time periods.***
Claim 15	**Claim 15**
15. The method of claim 14 further comprising providing a clock signal for performing said correlating step.	15. The method of claim 14 further ***comprising*** providing a clock signal for performing said correlating step.
Claim 16	**Claim 16**
16. The method of claim 15, wherein said disabling step	16. The method of claim 15, wherein said disabling step further ***comprises*** providing a signal to disable performance of said step of providing a clock

further comprises providing a signal to disable performance of said step of providing a clock signal.	signal.
Claim 21	**Claim 21**
21. The method of claim 14, wherein said disabling step further ***comprises*** defining a ***sampling window*** that encompasses said discrete time periods.	21. The method of claim 14, wherein said disabling step further ***comprises*** defining a ***sampling window*** [*a period of time during which a successful correlation is expected to occur*] that encompasses said ***discrete time periods.***

EXHIBIT B

UNITED STATES PATENT NUMBER 6.075.807-GLOSSARY OF TERMS

TERM	DEFINITION
AND gate	a ***logic gate*** whose output is true if and only if all of its inputs are true
bits	characters used to represent one of two digits in a system having two possible states, e.g., high or low, on or off, one or zero, +1 or -1, true or false, etc.
bit synchronization unit	a circuit that synchronizes the timing of the ***digital matched filter*** to the received signal
chips of said spreading code	the signals corresponding to the individual components of the spreading code
CMOS	a particular class of semiconductor
comprises	includes but is not limited to
comprising	including but not limited to
correlate	compare two signals to determine whether they agree or disagree
correlation	agreement or disagreement
correlation signal	a signal indicating ***correlation***
correlator	device which is capable of comparing two signals to determine whether they agree or disagree
coupled	operatively connected
digital delay line	See definition of "**digital delay line having a plurality of successive delay stages adapted to receive a multiple bit digital signal and propagate said digital signal therethrough at a fixed rate.**"
digital delay line having a plurality of successive delay stages adapted to receive a multiple bit digital signal and propagate said digital signal therethrough at a fixed rate	a device that moves a multiple bit digital signal through successive storage locations at a fixed rate. The multiple bit digital signal is delayed by being held in each storage location
discrete time periods	windows of time
exclusive-OR logic gates	logic gates whose outputs are true if either of one of its respective inputs, but not both inputs, is true

logic gates	basic electrical building blocks where the state of a logic gate's output is determined by the states of its inputs
plurality	two or more
propagating a received digital signal through a digital delay line having a plurality of successive delay stages	moving a digital signal through successive storage locations. The digital values are delayed by being held in each storage location
sampling window	a period of time during which a successful correlation is expected to occur
spreading code	a predetermined length sequence of chips that is used to modulate or 'spread' the signal before it is sent and that is used to demodulate or despread the signal after it is received

FN1. All terms appearing in bold face type and underlined have been construed by the court and appear with their definitions in the glossary in Exhibit B. The definition for each construed term appears in italics after its first use in the patent.

S.D.Cal.,2006.
Qualcomm Inc. v. Broadcom Corp.