United States District Court,
S.D. California.

QUALCOMM INCORPORATED,
Plaintiff.
v.
MAXIM INTEGRATED PRODUCTS, INC,
Defendants.
Maxim Integrated Products, Inc,
Counterclaimants.
v.
Qualcomm Incorporated,
Counterdefendant.

No. 02CV2429-B (JMA)

Nov. 7, 2005.

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CLAIM CONSTRUCTION ORDER FOR UNITED STATES PATENT NUMBER 6,615,027

RUDI M. BREWSTER**, Senior District Judge.**

Before the Court is the matter of claim construction for the asserted claims of United States Patent Number 6,615,027 ("the '027 Patent") in the above-titled patent infringement action. Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996), on April 12-13, 2005, the Court conducted a *Markman* hearing regarding construction of the disputed claim terms for the '027 Patent. Plaintiff Qualcomm, Inc. was represented by the law firm of Day, Casebeer, Madrid & Batchelder LLP, and Defendant Maxim Integrated Products, Inc. was represented by the firm of Perkins, Coie, Brown & Bain LLP.

The purpose of the Markman hearing was for the Court, with the assistance of the parties, to interpret the pertinent claims at issue in the '027 Patent. Additionally, the Court and the parties prepared a "case glossary" for this patent only, containing terms found in the claims and the specification for the '027 Patent, which are

considered to be technical in nature and which a jury of laypersons would not understand clearly without specific definition. As the case advances, the parties may request additional terms to be added to the glossary as to further facilitate the jury's understanding of the disputed claims.

After careful consideration of the parties' arguments and the applicable statutes and case law, the Court **HEREBY CONSTRUES** the claim terms in dispute in the '027 Patent and **ISSUES** the relevant jury instructions as written in Exhibit A, attached hereto. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED.

EXHIBIT A-UNITED STATES PATENT NUMBER 6,615,027-CLAIM CHART

Verbatim Patent Language	**Court's Claim Construction**
Claim 1.	Claim 1.
Circuitry to generate an interface signal between a first integrated circuit and a second integrated circuit comprising:	Circuitry to generate an **interface signal [a means of communication across a boundary]** between a first **integrated circuit [commonly referred to as a "chip," an integrated circuit is a combination of interconnected electrical components inseparably associated on or within a continuous piece of semiconductor material]** and a second integrated circuit **comprising [including but not limited to]:**
a reference circuit configured to provide a reference signal;	a reference **circuit [a network of electrical components connected directly or indirectly]** configured to provide a **reference signal [a benchmark signal against which something else can be compared];**
an interface circuit implemented on the first integrated circuit and operatively coupled to the reference circuit, the interface circuit configured to receive the reference signal and a data input and to generate the interface signal in response thereto; and	an interface circuit implemented on the first integrated circuit and operatively **coupled [associated in such a way that power or signal information may be transferred from one to another]** to the reference circuit, the interface circuit configured to receive the reference signal and a data input and to generate the interface signal in response thereto; and
a circuit element implemented on the second integrated circuit and operatively coupled to the interface circuit, the circuit element configured to receive the interface signal and provide an output signal in response,	a circuit element implemented on the second integrated circuit and operatively **coupled [associated in such a way that power or signal information may be transferred from one to another]** to the interface circuit, the **circuit element [a part of a circuit]** configured to receive the interface signal and provide an output signal in response,
wherein the interface signal is a differential current signal.	wherein the interface signal is a **differential current signal [a signal in which the information is conveyed through a difference in magnitude between two currents].**
Claim 2.	Claim 2.
The circuitry of claim 1, wherein the reference circuit is implemented on the second	The circuitry of claim 1, wherein the reference circuit is implemented on the second integrated circuit.

integrated circuit.	
Claim 3.	Claim 3.
The Circuitry of claim 1, further comprising:	The Circuitry of claim 1, further comprising:
at least one capacitor coupled between the differential current signal.	at least one **capacitor [a device capable of storing energy in the form of an electric field or charge] coupled between the differential current signal [coupled between the two conductors that make up the differential current signal].**
Claim 4.	Claim 14.
The circuitry of claim 1, wherein the interface signal represents an analog inphase (I) or quadrature (Q) baseband signal in a quadrature transmitter.	The circuitry of claim 1, wherein the interface signal represents an **analog inphase (I) or quadrature (Q) baseband signal [an analog signal is a signal in which the information content is expressed via a property of the signal, such as magnitude, frequency, amplitude and/or phase; a baseband signal is a signal with a band of frequencies occupied by the signal before it modulates the carrier (or subcarrier) frequency to form the transmitted line or radio signal; an inphase (I) baseband signal is a signal adapted to modulate an inphase carrier signal, i.e., one whose waves are synchronized in step with a timing reference; and a quadrature (Q) baseband signal is a signal adapted to modulate a quadrature phase carrier signal, i.e., one whose waves are 1/4 cycle (i.e., 90 degrees) out of synchronization with the waves of an inphase carrier signal]** in a **quadrature transmitter [a transmitter for transmitting signals that include inphase and quadrature signals].**
Claim 5.	Claim 5.
The circuitry of claim 1, wherein the reference signal is a voltage related to a bandgap voltage.	The circuitry of claim 1, wherein the reference signal is a voltage related to a **bandgap voltage [a voltage derived from the difference in energy between two specific electron energy bands of a semiconductor].**
Claim 6.	Claim 6.
The circuitry of claim 1, wherein the reference signal is a current generated from a reference voltage and a resistor.	The circuitry of claim 1, wherein the reference signal is a current generated from a reference voltage and a **resistor [a device whose primary function is resisting current flow].**
Claim 7.	Claim 7.
The circuitry of claim 6, wherein the output signal is a voltage signal, and wherein the resistor is external to the first and second integrated circuits.	The circuitry of claim 6, wherein the output signal is a **voltage signal [a signal in which information is conveyed through variations in voltage],** and wherein the resistor is external to the first and second integrated circuits.
Claim 8.	Claim 8.
The circuitry of claim 6, wherein the output signal is a current signal, and wherein the resistor is implemented on the second integrated circuit.	The circuitry of claim 6, wherein the output signal is a **current signal [a signal in which information is conveyed through variations in current],** and wherein the resistor is implemented on the second integrated circuit.
Claim 9.	Claim 9.

The circuitry of claim 6, wherein the interface circuit includes:	The circuitry of claim 6, wherein the interface circuit includes:
a current mirror configured to receive the reference signal and to provide two or more mirror paths, and	a **current mirror [a circuit capable of generating a signal whose current level is proportional to the current level of another signal]** configured to receive the reference signal and to provide two or more **mirror paths [paths for the flow of current generated by a current mirror],** and
a *switch array coupled to the current mirror,* the switching array configured to receive and decode the data input and to direct current from a set of selected mirror paths to an output of the switch array.	a ***switch array [a set of switches]*** coupled to the current mirror, the switching array configured to receive and decode the data input and to direct current from a set of selected mirror paths to an output of the switch array.
Claim 10.	Claim 10.
The circuitry of claim 1, wherein the data input comprises at least four bits of resolution.	The circuitry of claim 1, wherein **the data input comprises at least four bits of resolution [the data input has a resolution range of at least 16 possible values].**
Claim 11.	Claim 11.
The circuitry of claim 10, wherein the data input comprises at least eight bits of resolution.	The circuitry of claim 10, wherein the data input comprises at least **eight bits of resolution [the data input has a resolution range of at least 256 possible values].**
Claim 12.	Claim 12.
The circuitry of claim 1, wherein the interface circuit is oversampled by an oversampling ratio of two or greater.	The circuitry of claim 1, wherein the interface circuit is **oversampled [having a condition in which the values, or "samples," belonging to a digital signal are processed at a rate higher than necessary to accurately represent its analog form] by** an **oversampling ratio [the ratio of the sampling rate of a digital signal to the rate that is necessary to accurately represent its analog form]** of two or greater.
Claim 13.	Claim 13
The circuitry of claim 12, wherein the oversampling ratio is 16 or greater.	The circuitry of claim 12, wherein the oversampling ratio is 16 or greater.
Claim 14.	Claim 14.
The circuitry of claim 1, wherein the circuit element is a variable gain amplifier (VGA).	The circuitry of claim 1, wherein the circuit element is a **variable gain amplifier (VGA) [a unidirectional device that is capable of enlarging the waveform supplied to it, where the gain can be changed over a range, either continuously or in incremental steps].**
Claim 15.	Claim 15.
The circuitry of claim 1, wherein the circuit element is a modulator.	The circuitry of claim 1, wherein the circuit element is a **modulator [a device capable of combining an information signal with a carrier signal].**
Claim 16.	Claim 16.
The circuitry of claim 15,	The circuitry of claim 15, wherein the modulator includes

wherein the modulator includes	
a pair of current sources coupled to the interface signal, and	a pair of **current sources [a device for providing a current at a specified value] coupled [associated in such a way that power or signal information may be transferred from one to another]** to the **interface signal [a means of communication across a boundary],** and
a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers configured to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the interface signal.	a pair of **cross-coupled [having the condition in which the "positive" output of one differential device is coupled to the "negative" output of another differential device, and vice versa]** differential amplifiers, each **differential amplifier [an amplifier whose output signal is proportional to the difference between two input signals] coupled [associated in such a way that power or signal information may be transferred from one to another]** to a respective current source, the differential amplifiers configured to receive a carrier signal and to generate the output signal based, in part, on the **carrier signal [a signal of a single frequency capable of being modulated by an information signal]** and the **interface signal [a means of communication across a boundary].**
Claim 17.	Claim 17.
The circuitry of claim 16, wherein each current source in the modulator provides a bias current that is related to the reference signal.	The circuitry of claim 16, wherein each current source in the modulator provides a **bias current [a current delivered to a circuit or device for establishing its operating point]** that is related to the reference signal.
Claim 18.	Claim 18.
A transmitter comprising the circuitry of claim 1.	A transmitter comprising the circuitry of claim 1.
Claim 19	Claim 19
A transmitter in a CDMA cellular telephone comprising the circuitry of claim 1.	A transmitter in a **CDMA [an acronym for Code Division Multiple Access, a digital communication technique that uses codes to separate users' information]** cellular telephone comprising the circuitry of claim 1.
Claim 20.	Claim 20.
Circuitry in a transmitter comprising:	Circuitry in a transmitter comprising:
a first interface circuit implemented on a first integrated circuit, the first interface circuit configured to receive a first data input and provide a first differential current signal; and	a first interface circuit implemented on a first integrated circuit, the first interface circuit configured to receive a first data input and provide a first differential current signal; and
a modulator implemented on a second integrated circuit and operatively coupled to the first interface circuit, the modulator configured to receive the first differential current signal and a carrier signal and to generate an	a modulator implemented on a second integrated circuit and operatively coupled to the first interface circuit, the modulator configured to receive the first differential current signal and a carrier signal and to generate an output signal in response thereto.

output signal in response thereto.	
Claim 21.	Claim 21.
The circuitry of claim 20, further comprising:	The circuitry of claim 20, further comprising:
a second interface circuit implemented on the first integrated circuit, the second interface circuit configured to receive a second data input and provide a second differential current signal,	a second interface circuit implemented on the first integrated circuit, the second interface circuit configured to receive a second data input and provide a second differential current signal,
wherein the modulator is further configured to receive the second differential current signal and to generate the output signal in response to the second differential current signal.	wherein the modulator is further configured to receive the second differential current signal and to generate the output signal in response to the second differential current signal.
Claim 22.	Claim 22.
The circuitry of claim 21, wherein the first and second data inputs correspond to inphase (I) and quadrature (Q) baseband signals in a quadrature transmitter.	The circuitry of claim 21, wherein the first and second data inputs correspond to inphase (I) and quadrature (Q) baseband signals in a quadrature transmitter.
Claim 23.	Claim 23.
The circuitry of claim 21, further comprising:	The circuitry of claim 21, further comprising:
a capacitor coupled between each of the first and second differential current signals.	a capacitor coupled between each of the first and second differential current signals.
Claim 24.	Claim 24.
The circuitry of claim 21, wherein each of the first and second data inputs has eight or more bits of resolution.	The circuitry of claim 21, wherein each of the first and second data inputs has **eight or more bits of resolution [the data input has a resolution range of at least 256 possible values].**
Claim 25.	Claim 25.
The circuitry of claim 21, wherein the first and second interface circuits are operated at an oversampled rate relative to a rate of the first and second data inputs.	The circuitry of claim 21, wherein the first and second interface circuits are operated at an oversampled rate relative to a rate of the first and second data inputs.
Claim 26.	Claim 26.
The circuitry of claim 25,	The circuitry of claim 25, wherein the oversampled rate is sixteen or

wherein the oversampled rate is sixteen or greater.	greater.
Claim 27.	Claim 27.
The circuitry of claim 20, further comprising:	The circuitry of claim 20, further comprising:
a reference circuit implemented on the second integrated circuit and configured to provide a reference signal,	a reference circuit implemented on the second integrated circuit and configured to provide a reference signal,
wherein the first interface circuit couples to the reference circuit and is further configured to receive the reference signal and to generate the first differential current signal based, in part, on the reference signal.	wherein the first interface circuit couples to the reference circuit and is further configured to receive the reference signal and to generate the first differential current signal based, in part, on the reference signal.
Claim 28.	Claim 28.
The circuitry of claim 27, wherein the reference signal is a current generated based on a reference voltage.	The circuitry of claim 27, wherein the reference signal is a current generated based on a reference voltage.
Claim 29	Claim 29
A transmitter in a cellular telephone comprising:	A transmitter in a cellular telephone comprising:
a digital processor implemented on a first integrated circuit and configured to provide digital inphase (I) and quadrature (Q) baseband signals;	a digital processor implemented on a first integrated circuit and configured to provide digital inphase (I) and quadrature (Q) baseband signals;
first and second interface circuits implemented on the first integrated circuit and coupled to the digital processor, each interface circuit configured to receive a respective digital baseband signal and provide an analog baseband signal, wherein each quantized analog baseband signal comprises at least four bits of resolution and is implemented as a differential current signal; and	first and second interface circuits implemented on the first integrated circuit and coupled to the digital processor, each interface circuit configured to receive a respective digital baseband signal and provide an analog baseband signal, wherein each **quantized [subdivided into non-overlapping intervals, with a discrete value assigned to each subdivision] analog baseband signal comprises at least four bits of resolution [the analog baseband signal has a resolution range of at least 16 possible values]** and is implemented as a differential current signal; and
a modulator implemented on a second integrated circuit and operatively coupled to the first	a modulator implemented on a second integrated circuit and operatively coupled to the First and second interface circuits, the modulator configured to receive and **modulate [to combine an information signal with a**

and second interface circuits, the modulator configured to receive and modulate the analog baseband signals with a carrier signal to provide a modulated output signal.	**carrier signal]** the analog baseband signals with a carrier signal to provide a modulated output signal
Claim 30.	Claim 30.
The transmitter of claim 29, further comprising:	The transmitter of claim 29, further comprising:
a reference circuit implemented on the second integrated circuit and configured to provide a reference signal,	a reference circuit implemented on the second integrated circuit and configured to provide a reference signal,
wherein each interface circuit couples to the reference circuit and is further configured to receive the reference signal, and wherein the analog baseband signals are further generated-based, in part, on the reference signal.	wherein each interface circuit couples to the reference circuit and is further configured to receive the reference signal, and wherein the analog baseband signals are further generated based, in part, on the reference signal.
Claim 31.	Claim 31.
A device comprising:	A device comprising:
an interface circuit formed on a first integrated circuit (IC) for generating a differential current signal responsive to a reference signal and to a digital data input; and	an interface circuit formed on a first integrated circuit (IC) for generating a differential current signal responsive to a reference signal and to a digital data input; and
a circuit element formed on a second IC for generating an output signal on the basis of the differential current signal.	a circuit element formed on a second IC for generating an output signal on the basis of the differential current signal.
Claim 32.	Claim 32.
The device of claim 31, wherein the device is a transmitter.	The device of claim 31, wherein the device is a transmitter.
Claim 33.	Claim 33.
The device of claim 32, wherein the transmitter is a quadrature transmitter.	The device of claim 32, wherein the transmitter is a quadrature transmitter.
Claim 34.	Claim 34.
The device of claim 31, wherein the device is a CDMA telephone.	The device of claim 31, wherein the device is a CDMA telephone.
Claim 35.	Claim 35.
The device of claims 31, 32, or	The device of claims 31, 32, or 34, wherein the reference signal is generated

34, wherein the reference signal is generated by a reference circuit on the second IC.	by a reference circuit on the second IC.
Claim 36.	Claim 36.
The device of claims 31, 32, or 34, further comprising a reference circuit for generating the reference signal.	The device of claims 31, 32, or 34, further comprising a reference circuit for generating the reference signal.
Claim 37.	Claim 37.
The device of claims 31, 32, or 34, further comprising at least one capacitor coupled between the differential current signal.	The device of claims 31, 32, or 34, further comprising at least one capacitor coupled between the differential current signal.
Claim 38.	Claim 38.
The device of claims 31, 32, or 34, wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.	The device of claims 31, 32, or 34, wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.
Claim 41.	Claim 41.
The device of claims 31, 32, or 34, wherein the reference signal is a current generated from a reference voltage and a resistor.	The device of claims 31, 32, or 34, wherein the reference signal is a current generated from a reference voltage and a resistor.
Claim 42.	Claim 42.
The device of claim 41, wherein the output signal is a voltage signal and the resistor is external to the first and second ICs.	The device of claim 41, wherein the output signal is a voltage signal and the resistor is external to the first and second ICs.
Claim 43.	Claim 43.
The device of claim 41, wherein the output signal is a current signal and resistor is implemented on the second IC.	The device of claim 41, wherein the output signal is a current signal and resistor is implemented on the second IC.
Claim 44.	Claim 44.
The device of claims 31, 32, or 34, wherein the interface circuit includes a current mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current	The device of claims 31, 32, or 34, wherein the interface circuit includes a current mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.

signal.	
Claim 45.	Claim 45.
The device of claims 31, 32, or 34, wherein the digital data input is at least a four bit digital data input.	The device of claims 31, 32, or 34, wherein the digital data input is at least a **four bit [four binary values of zeros or ones to identify sixteen separate values] digital data input.**
Claim 46.	Claim 46.
The device of claims 31, 32, or 34, wherein the digital data input is an oversampled digital data signal.	The device of claims 31, 32, or 34, wherein the digital data input is an oversampled digital data signal.
Claim 47.	Claim 47.
The device of claims 31, 32, or 34, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.	The device of claims 31, 32, or 34, wherein the circuit element is any of a variable gain amplifier (VGA), **mixer [a device capable of converting an input signal to a different frequency range in response to an oscillating signal],** and **power amplifier (PA) driver [a device capable of supplying a signal that meets the minimum input power requirements of a power amplifier].**
Claim 48.	Claim 48.
The device of claims 31, 32, or 34, wherein the circuit element is a modulator.	The device of claims 31, 32, or 34, wherein the circuit element is a modulator.
Claim 49.	Claim 49.
The device of claim 48, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.	The device of claim 48, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.
Claim 50.	Claim 50.
The device of claim 49, wherein each current source in the modulator provides a bias current that is related to the reference signal.	The device of claim 49, wherein each current source in the modulator provides a bias current that is related to the reference signal.
Claim 51.	Claim 51.
The device of claim 48, wherein the modulator performs direct	The device of claim 48, wherein the modulator performs **direct up conversion [converting an information signal to an output signal having**

up conversion.	**a higher frequency that is suitable for radio transmission, without first converting the information signal to an output signal having an intermediate frequency].**
Claim 52.	Claim 52.
A device comprising:	A device comprising:
an interface circuit for generating a differential current signal, responsive to a reference signal and to a digital data input and adapted for external capacitive filtering between the differential current signal; and	an interface circuit for generating a differential current signal, responsive to a reference signal and to a digital data input and adapted for external **capacitive filtering [use of a capacitor to suppress portions of an inputted signal so that desired frequencies are passed through and other frequencies are suppressed] between the differential current signal [between the two conductors that make up the differential current signal];** and
a circuit element for generating an output signal on the basis of the differential current signal.	a circuit element for generating an output signal on the basis of the differential current signal.
Claim 53.	Claim 53.
The device of claim 52, wherein the device is a transmitter.	The device of claim 52, wherein the device is a transmitter.
Claim 54.	Claim 54.
The device of claim 53, wherein the transmitter is a quadrature transmitter.	The device of claim 53, wherein the transmitter is a quadrature transmitter.
Claim 55.	Claim 55.
The device of claim 52, wherein the device is a CDMA telephone.	The device of claim 52, wherein the device is a CDMA telephone.
Claim 56.	Claim 56.
The device of claims 52, 53, or 55, wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.	The device of claims 52, 53, or 55, wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.
Claim 57.	Claim 57.
The device of claims 52, 53, or 55, wherein the interface circuit includes a current mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.	The device of claims 52, 53, or 55, wherein the interface circuit includes a current mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.
Claim 58.	Claim 58.
The device of claims 52, 53, or	The device of claims 52, 53, or 55, wherein the circuit element is any of a

55, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.	variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.
Claims 59.	Claims 59.
The device of claims 52, 53, or 55, wherein the circuit element is a modulator.	The device of claims 52, 53, or 55, wherein the circuit element is a modulator.
Claim 60.	Claim 60.
The device of claim 54, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.	The device of claim 54, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.
Claim 61.	Claim 61.
The device of claim 60, wherein each current source in the modulator provides a bias current that is related to the reference signal.	The device of claim 60, wherein each current source in the modulator provides a bias current that is related to the reference signal.
Claim 62.	Claim 62.
The device of claim 60, wherein the modulator performs direct up conversion.	The device of claim 60, wherein the modulator performs direct up conversion.
Claim 63.	Claim 63.
An analog integrated circuited (IC) adapted for use in a transmit signal path of a communication device, and responsive to an input differential current signal generated externally as a function of a reference signal and a digital data input, the analog IC comprising: a reference circuit for generating the	An analog integrated circuited (IC) adapted for use in a **transmit signal path [circuitry through which a transmit signal can flow]** of a communication device,[FN1] and **responsive to an input differential current signal [capable of accepting an input differential current signal and capable of taking some action in response]** generated externally as a function of a reference signal and a digital data input, the analog IC comprising: a reference circuit for generating the reference signal; and a circuit element for generating an output signal on the basis of **the differential current signal [the input differential current signal].**

reference signal; and a
circuit element for
generating an output signal
on the basis of the
differential current signal.

FN1. The preceding portion of claim 63 is introductory language that does not limit the scope of the claim.

Claim 66.	Claim 66.
The analog integrated circuit of claim 63, wherein the reference signal is a current generated from a reference voltage and a resistor.	The analog integrated circuit of claim 63, wherein the reference signal is a current generated from a reference voltage and a resistor.
Claim 67.	Claim 67.
The analog integrated circuit of claim 66, wherein the output signal is a voltage signal and the resistor is external to the analog integrated circuit.	The analog integrated circuit of claim 66, wherein the output signal is a voltage signal and the resistor is external to the analog integrated circuit.
Claim 68.	Claim 68.
The analog integrated circuit of claim 66, wherein the output signal is a current signal and the resistor is implemented on the analog integrated circuit.	The analog integrated circuit of claim 66, wherein the output signal is a current signal and the resistor is implemented on the analog integrated circuit.
Claim 69.	Claim 69.
The analog integrated circuit of claim 63, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.	The analog integrated circuit of claim 63, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.
Claim 70.	Claim 70.
The analog integrated circuit of claim 63, wherein the circuit element is a modulator.	The analog integrated circuit of claim 63, wherein the circuit element is a modulator.
Claim 71.	Claim 71.
The analog integrated circuit of claim 70, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.	The analog integrated circuit of claim 70, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.
Claim 72.	Claim 72.
The analog integrated circuit of claim 71, wherein each current source in a modulator provides a bias current that is related to the reference signal.	The analog integrated circuit of claim 71, wherein each current source in a modulator provides a bias current that is related to the reference signal.
Claim 73.	Claim 73.
The analog integrated circuit of claim 70, wherein the modulator performs direct up conversion.	The analog integrated circuit of claim 70, wherein the modulator performs direct up conversion.
Claim 78.	Claim 78.

A method comprising:	A method comprising:
generating a reference signal;	generating a reference signal;
providing the reference signal to a first circuit;	providing the reference signal to a first circuit;
receiving a digital data input at the first circuit;	receiving a digital data input at the first circuit;
generating a differential current signal in the first circuit based, in part, on the digital data input and the reference signal;	generating a differential current signal in the first circuit based, in part, on the digital data input and the reference signal;
providing the differential current signal from the first circuit to a second circuit;	providing the differential current signal from the first circuit to a second circuit;
receiving the differential current signal at the second circuit; and	receiving the differential current signal at the second circuit; and
generating an output signal from a circuit element in the second circuit, the output signal being based at least in part on the differential current signal.	generating an output signal from a circuit element in the second circuit, the output signal being based at least in part on the differential current signal.
Claim 79.	Claim 79.
The method of claim 78, wherein the reference signal is a current generated from a reference voltage.	The method of claim 78, wherein the reference signal is a current generated from a reference voltage.
Claim 80.	Claim 80.
The method of claim 78, further comprising filtering the differential current signal.	The method of claim 78, further comprising **filtering [suppressing portions of an inputted signal so that desired frequencies are passed through and other frequencies are suppressed]** the differential current signal.
Claim 81. The method of claim 78, further comprising providing a signal related to the reference signal to the circuit element, wherein the output signal is further generated based, in part, on the signal related to the reference signal.	Claim 81. The method of claim 78, further comprising providing a signal related to the reference signal to the circuit element, wherein the output signal is further generated based, in part, on the signal related to the reference signal.

EXHIBIT B-GLOSSARY RE: UNITED STATES PATENT NUMBER 6,615,027

Term	Definition
analog baseband signal comprises at least four bits of resolution	the analog baseband signal has a resolution range of at least 16 possible values
analog inphase (I) or quadrature (Q) baseband signal	an analog signal is a signal in which the information content is expressed via a property of the signal, such as magnitude, frequency, amplitude and/or phase; a baseband signal is a signal with a band of frequencies occupied by the signal before it modulates the carrier (or subcarrier) frequency to form the transmitted line or radio signal; an inphase (I) baseband signal is a signal adapted to modulate an inphase carrier signal, i.e., one whose waves are synchronized in step with a timing reference; and a quadrature (Q) baseband signal is a signal

	adapted to modulate a quadrature phase carrier signal, i.e., one whose waves are 1/4 cycle (i.e., 90 degrees) out of synchronization with the waves of an inphase carrier signal
bandgap voltage	a voltage derived from the difference in energy between two specific electron energy bands of a semiconductor
between the differential current signal	between the two conductors that make up the differential current signal
bias current	a current delivered to a circuit or device for establishing its operating point
capacitor	a device capable of storing energy in the form of an electric field or charge
capacitive filtering	use of a capacitor to suppress portions of an inputted signal so that desired frequencies are passed through and other
carrier signal	a signal of a single frequency capable of being modulated by an information signal
CDMA	an acronym for Code Division Multiple Access, a digital communication technique that uses codes to separate users' information
circuit	a network of electrical components connected directly or indirectly
circuit element	a part of a circuit
comprising	including but not limited to
coupled	associated in such a way that power or signal information may be transferred from one to another
coupled between the differential current signal	coupled between the two conductors that make up the differential current signal
cross-coupled	having the condition in which the "positive" output of one differential device is coupled to the "negative" output of another differential device, and vice versa
current mirror	a circuit capable of generating a signal whose current level is proportional to the current level of another signal
current signal	a signal in which information is conveyed through variations in current
current sources	a device for providing a current at a specified value
differential amplifier	an amplifier whose output signal is proportional to the difference between two input signals
differential current signal	a signal in which the information is conveyed through a difference in magnitude between two currents
the differential current signal (for claim 63)	the input differential current signal
direct up conversion	converting an information signal to an output signal having a higher frequency that is suitable for radio transmission, without first converting the information signal to an output signal

	having an intermediate frequency
eight bits of resolution	the data input has a resolution range of at least 256 possible values
eight or more bits of resolution	the data input has a resolution range of at least 256 possible values
filtering	suppressing portions of an inputted signal so that desired frequencies are passed through and other frequencies are suppressed
four bit	four binary values of zeros or ones to identify sixteen separate values
four bits of resolution	a resolution range of 16 possible values
integrated circuit	commonly referred to as a "chip," an integrated circuit is a combination of interconnected electrical components inseparably associated on or within a continuous piece of semiconductor material
interface signal	a means of communication across a boundary
mirror paths	paths for the flow of current generated by a current mirror
mixer	a device capable of converting an input signal to a different frequency range in response to an oscillating signal
modulate	to combine an information signal with a carrier signal
modulator	a device capable of combining an information signal with a carrier signal
oversampled	having a condition in which the values, or "samples" belonging to a digital signal are processed at a rate higher than necessary to accurately represent its analog form
oversampling ratio	the ratio of the sampling rate of a digital signal to the rate that is necessary to accurately represent its analog form
power amplifier (PA) driver	a device capable of supplying a signal that meets the minimum input power requirements of a power amplifier
reference signal	a benchmark signal against which something else can be compared
resistor	a device whose primary function is resisting current flow
responsive to an input differential current signal	capable of accepting an input differential current signal and capable of taking some action in response
quadrature transmitter	a transmitter for transmitting signals that include inphase and quadrature signals
quantized	subdivided into non-overlapping intervals, with a discrete value assigned to each subdivision
switch array	a set of switches
transmit signal path	circuitry through which a transmit signal can flow
variable gain amplifier (VGA)	a unidirectional device that is capable of enlarging the waveform supplied to it, where the gain can be changed over a range, either continuously or in incremental steps
voltage	a signal in which information is conveyed through variations in voltage

signal

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