United States District Court,
D. Delaware.

NEOMAGIC CORPORATION,
Plaintiff.
v.
TRIDENT MICROSYSTEMS, INC,
Defendant.

No. CIV. A. 98-699-RRM

May 8, 2000.

In construing disputed claims of patents directed to a graphics controller used in notebook computers, the District Court, McKelvie, J., held that: (1) term "power supply" referred to a source of electrical energy, such as a battery, that required at least two power supply lines to deliver power in an electrical circuit; (2) term "logic gates" referred to the logic circuitry that makes up the graphics engine and manipulates video data on a computer screen; and (3) term "memory portion" referred to the circuitry required for a working memory, including the memory cells that store data and the circuitry associated with reading, writing, addressing and refreshing data in the memory cells.

Terms construed.

5,650,955, 5,703,806. Cited.

Richard L. Horwitz, Joanne Ceballos, William J. Dorgan, Potter Anderson & Corroon LLP, Wilmington, DE, R.V. Lupo, Jack Q. Lever, Jr., Donna M. Tanguay, Brian E. Ferguson, Raymond A. Jacobsen, Jr., Stephen K. Shahida, McDermott, Will & Emery, Washington, DC, Steven A. Maddox, McDermott, Will & Emery, Menlo Park, CA, for plaintiff.

Donald F. Parsons, Jr.,Mary B. Graham, Lisa K.W. Crossland, Morris, Nichols, Arsht & Tunnell, Wilmington, DE, James Pooley, Ian N. Feinberg, Barry N. Young, Elizabeth Day, Gray Cary Ware & Freidenrich LLP, Palo Alto, CA, for defendant.

OPINION

McKELVIE**, District Judge.**

This is a patent case. Plaintiff NeoMagic Corporation is a Delaware corporation with its principal place of business in Santa Clara, California. NeoMagic is the owner of U.S. Patent Nos. 5,650,955 (the '955 patent) and 5,703,806 (the '806 patent) which are directed to a graphics controller used in notebook computers. Defendant Trident Microsystems, Inc. is a Delaware corporation with its principal place of business in

Mountain View, California.

On December 14, 1998, NeoMagic filed a complaint alleging that Trident infringes one or more claims of the '955 and '806 patents. Trident filed its answer on January 25, 1999, in which it denied NeoMagic's allegation of infringement and asserted affirmative defenses of invalidity and unenforceability. On the same day, Trident filed an antitrust counterclaim against NeoMagic pursuant to section 2 of the Sherman Act, 15 U.S.C. s. 2. The case is scheduled for a ten-day jury trial beginning July 31, 2000.

On April 13, 2000, the court held a trial in accordance with Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), to construe disputed claims of the '955 and '806 patents.This is the court's construction of those disputed claims.

I. *FACTUAL AND PROCEDURAL BACKGROUND*

The court draws the following facts from the affidavits, documents and deposition transcripts submitted by the parties.

A. *General Description of the Technology*

The patents in suit relate to technology for displaying graphics on computer screens. In computers, devices commonly known as "graphics controllers" manipulate the video data that is displayed on the computer screen. A graphics controller has two main components, a graphics engine and video memory.

The graphics engine in the controller consists of logic circuitry that manipulates the video data for graphics operations. Logic circuitry refers to gates, flip-flops and other on/off circuits used to perform problem-solving functions in a computer. The graphics engine receives the video data from the computer's central processing unit ("CPU"), processes the data, and stores the data in the video memory. The graphics engine also regularly retrieves processed data from the video memory and feeds that data to the computer screen.

The video memory in the graphics controller typically consists of one or more conventional memory chips, such as dynamic random access memory ("DRAM") chips. DRAM chips are made up of memory cells and a small amount of logic circuitry. The video memory in the graphics controller is separate from other memory in the computer which may also consist of DRAM chips.

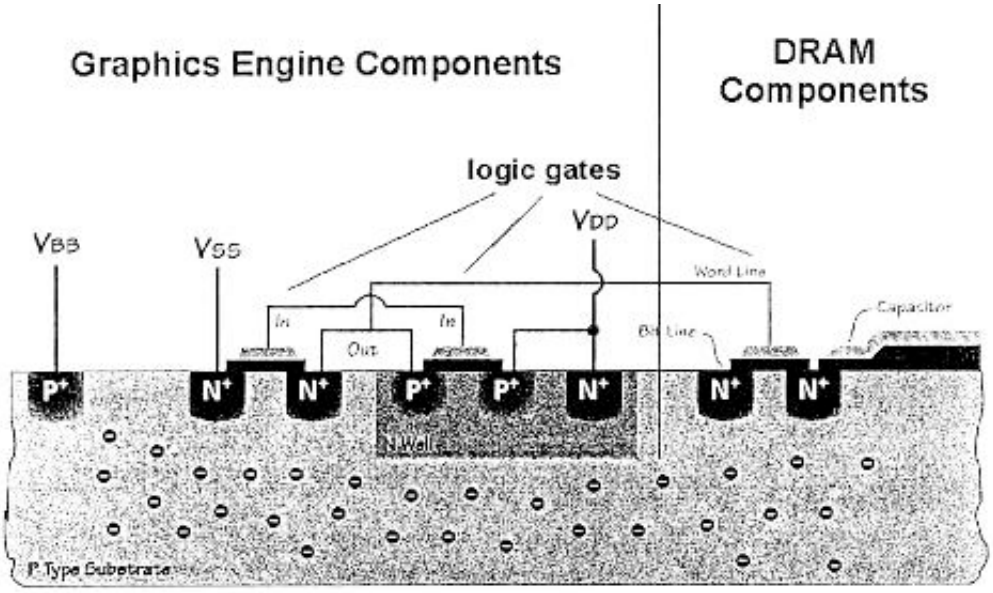
Prior to 1993, the graphics engine and the video memory were separate components in the graphics controller. A typical graphics controller consisted of at least five chips: one chip for the graphics engine and four separate DRAM chips for the video memory. This design had two major disadvantages, particularly for notebook computers. First, the graphics controller took up more internal "board" space in the notebook computer because the controller contained several discrete chips. Second, because each additional chip requires more power, the graphics controller created a significant drain on the battery power in a notebook computer.

In 1993, NeoMagic set out to improve the quality of graphics in notebook computers by designing a graphics controller with the graphics engine and the video memory combined on a single chip. A single chip graphics controller was desirable because it would consume less power and take up less board space. In order to put the high-speed logic of the graphics engine on the same chip with the DRAM, however, NeoMagic had to eliminate "noise" and "latch-up."

Noise refers to excess charge carriers that escape from the high-speed logic circuitry of the graphics engine and collect in the silicon substrate of the graphics controller chip. Each time charge carriers flow through a logic gate, some of the charge carriers leak into the substrate. When this happens, the charge carriers may "latch-up" and open a conductive path in the substrate between the source and drain terminals of the logic gates. This causes a charge to flow through the substrate where it was never intended to flow.

The following illustration, which was submitted by Trident at the *Markman* trial, helps explain the problem of noise and latch-up. The illustration represents a horizontal cross section of a graphics controller chip with the graphics engine and video memory combined on the same silicon substrate. The N+ and P+ logic gates on the left side of the substrate make up an inverter from a graphics engine. The N+ logic gate and the capacitor on the right side of the substrate are standard DRAM components. V_{SS} and V_{DD} represent source and drain terminals and the voltage applied to the substrate is referred to as V_{BB}.

***541**



The charge carriers pictured in the pictured in the substrate beneath the graphics engine and memory portions represent noise. When logic and memory are combined on the same substrate, the charge carriers may latch-up and create disturbances. The disturbances may appear as visible patterns on the computer screen. Deepraj S. Puar, one of NeoMagic's founders, testified during a deposition that noise and latch-up were two of the major problems that NeoMagic's inventors had to solve while designing the integrated graphics controller.

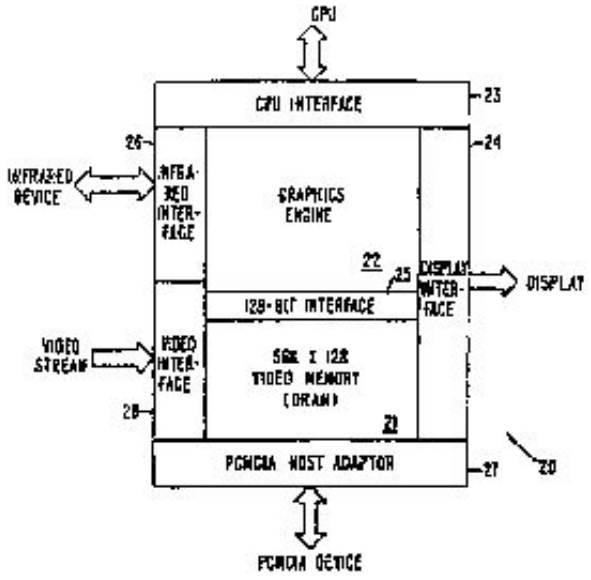
B. *The '955 and* '806 Patents

On July 22, 1997, the United States Patent and Trademark Office ("PTO") issued the '955 patent to NeoMagic as assignee of the inventors, Deepraj Puar and Ravi Ranganathan. Less than six months later, on December 30, 1997, the PTO issued the '806 patent to NeoMagic as assignee of the inventors Puar and

Ranganathan. The '955 and '806 patents share a common specification and both are entitled "Graphics Controller Integrated Circuit Without Memory Interface."

The '955 and '806 patents describe a graphics controller that integrates the graphics engine and the video memory onto a single chip. Figure 2 of the '955 and '806 patents, which is reproduced below, illustrates the general organization of a graphics controller integrated circuit according to the invention.

***542**



The invention is also referred to as a "single chip graphics controller with embedded memory." The specification of the '955 and '806 patents states:

In accordance with the present invention, the graphics controller functions are integrated on the same integrated circuit substrate as the video memory, as shown in FIG. 2. A single integrated circuit has a portion of its substrate for an advanced graphics engine, the circuitry which handles the graphics controller functions and manipulates the video data. The integrated circuit also has another portion of the substrate for a video memory in the form of a DRAM.

In the specification of the '955 and '806 patents, the inventors also describe their solution to noise and latch-up. According to the invention, noise and latch-up are minimized by applying a voltage to the substrate to draw the charge carriers in the substrate away from the logic and memory portions. The specification provides:

The logic circuits of the integrated circuit are redesigned to decouple the V_{SS} line connected to the source terminals of the N-channel pulldown transistors from the P-substrate tap. As shown in FIG. 4, the source of the N-channel, pulldown transistor 35 of a representational logic circuit is connected to a V_{SS} line 45 (at 0 volts), while the substrate is tapped by a V_{BB} line 47 (at -1.5 volts).

Figure 4 of the '955 and '806 patents, which is reproduced below, is a circuit diagram of an inverter connected according to the invention in an integrated circuit.

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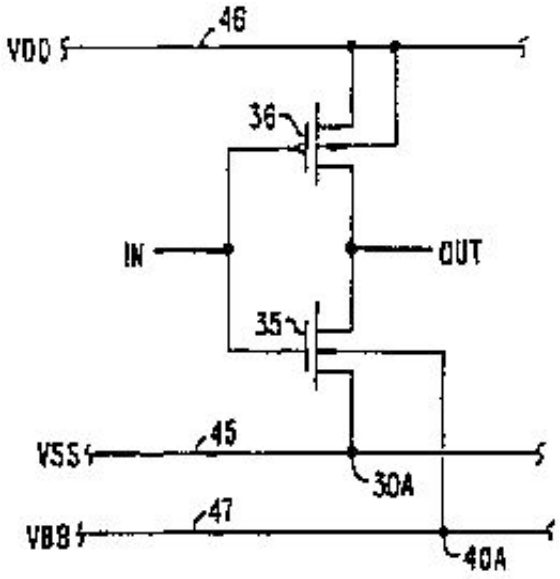
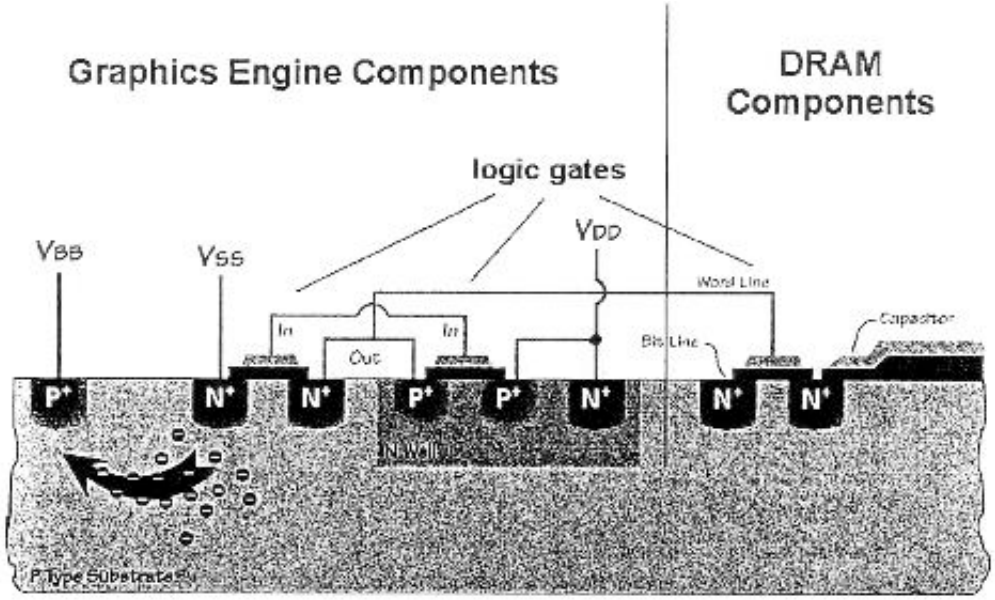


NeoMagic and Trident refer to this process as "reverse-biasing" the substrate. The following illustration, which was submitted by Trident at the *Markman* trial, helps explain how reverse-biasing the substrate solves the noise and latch-up problem. The illustration represents a horizontal cross section of a graphics controller chip with the graphics engine and video memory combined on the same silicon substrate. As before, the N+ and P+ logic gates on the left side of the substrate make up an inverter from a graphics engine. The N+ logic gate and the capacitor on the right side of the substrate are standard DRAM components. V_{SS} and V_{DD} represent source and drain terminals and the voltage applied to the substrate is referred to as V_{BB}.



As provided in the specification, the negative 1.5 volts applied to the substrate, V_{BB}, causes excess charge carriers in the substrateto flow away from the logic and memory portions of the graphics controller.

C. ***Prosecution History of the '955 and*** '806 Patents

The '955 and '806 patents issued from continuation applications based on a June 20, 1994 parent application that was subsequently abandoned.

1. ***Parent Application of June 20, 1994***

On June 20, 1994, inventors Puar and Ranganathan applied for a patent for a graphics controller integrated circuit. In their application, the inventors describe a graphics controller system with increased performance and reduced power dissipation. The application states that the invention provides for "particular arrangements for logic circuits and output buffer circuits so that large amounts of logic circuitry sufficient to perform graphics controller system functions may be integrated with the large amounts of memory sufficient to act as high performance video memory." As it was originally submitted, the application contained eleven claims.

Claim 10, as submitted in the parent application, reads:

10. An integrated circuit comprising

a logic portion having at least 30K logic gates; and

a memory portion having a capacity of at least 2 megabits.

On August 15, 1994, before the PTO examined their application, Puar and Ranganathan filed a preliminary amendment to add Claims 12-24. The inventors wrote that the additional claims were needed to more completely claim the subject matter of their invention. According to the proposed amendment, "Claim 12

covers a logic circuit, claim 17[a] buffer circuit and Claim 21 a capacitor in accordance with various aspects of the applicants' invention."

Claim 18, as submitted in the proposed amendment, reads:

18. (New) A buffer circuit of claim 17 wherein first power supply is at approximately +5 volts, said second power supply at approximately 0 volts and said third power supply at +6 volts.

Claim 21, as submitted in the proposed amendment, reads:

21. (New) In an integrated circuit having a logic portion having at least 30K logic gates and a memory portion having a capacity of at least 2 megabits, a capacitor comprising

a PMOS transistor in an N-well in a semiconductor substrate, said PMOS transistor having a gate, first and second source/drains, said first source/drain connected in common to said second source/drain to form a first terminal of said capacitor, said gate forming a second terminal of said capacitor, said N-well connected to a first power supply, and said substrate connected to a second power supply at a negative voltage with respect to said first power supply;

whereby said capacitor is isolated from electrical noise in said substrate.

2. ***Rejection of October 5, 1995***

On October 5, 1995, the examiner rejected Claims 1-24. The examiner issued a restriction requirement because he found that the claims were directed to more than one invention. According to the examiner, Claims 1-9 and 12-20 were drawn to memory and power conservation, while Claims 10-11 and 21-24 were drawn to an integrated circuit. FN1 The examiner directed the inventors to elect a single invention.

FN1. In the rejection of October 5, 1995, the examiner mistakenly wrote that "Claims 11 and 12-24" were drawn to an integrated circuit. The inventors corrected this mistake in their January 2, 1996 amendment.

The examiner also rejected Claims 1-24 on their merits. Claim 10 was rejected as indefinite under 35 U.S.C. s. 112 because there was "no indication claimed of any interconnection." FN2 Claim 10 was further rejected pursuant to 35 U.S.C. s. 102 as anticipated by an electronic parts catalog. FN3 Claims 10, 11 and 21-24 were rejected under s. 102 as anticipated by U.S. Patent No. 5,323,343 which issued June 21, 1994 to I. Ogoh. Finally, Claims 1-9 were rejected under s. 102 as anticipated by U.S. Patent No. 5,434,969 which issued in July, 1995 to Heilveil. According to the examiner, "Heilveil teaches a video memory controlled by a centered processor."

FN2. 35 U.S.C. s. 112, para. 6 provides:
An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

FN3. 35 U.S.C. s. 102 provides, in pertinent part:
A person shall be entitled to a patent unless-

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent ....

3. ***Amendment of January 2, 1996***

On January 2, 1996, Puar and Ranganathan submitted an amendment and response to the PTO's restriction requirement. The inventors canceled Claims 1-9 and 11-20 and elected to prosecute Claims 10 and 21-24. In addition, the inventors added Claims 25-50 to more fully claim the invention. Claims 25-32 were dependent on Claim 10 and Claims 33-39 were dependent on Claim 21.

Claim 10, as submitted in the proposed amendment, reads as follows, with the underlining indicating added language:

10. (Once amended) An integrated circuit comprising a logic portion having at least 30K logic gates; and a memory portion *interconnected with said logi* capacity of at least 2 megabits.

Puar and Ranganathan proposed amending Claim 10 in this manner to overcome the examiner's rejection for indefiniteness because the claim had "no indication claimed of any interconnection." The inventors disagreed with the examiner that Claim 10 was anticipated by an electronic parts catalog. According to the inventors, an integrated circuit is not an electronics part catalog. Furthermore, the inventors wrote that Claim 10 recites that the logic portion is interconnected with the memory portion and an electronic parts catalog has no such interconnection.

Claim 21, as submitted in the proposed amendment, reads as follows, with the underlining and brackets indicating added and retracted language, respectively:

21. (Once amended) In an integrated circuit having a logic portion having at least 30K logic gates and a memory portion *coupled to said logic portion, said memory portion* having a capacity of at least 2 megabits, a capacitor comprising

a [PMOS] *first dopant-type* transistor in an [N-well] *a second dopant-type well* in a *first dopant-type* semiconductor substrate, said [PMOS] *first dopant-type* transistor having a gate, first and second source/drains, said first source/drain connected in common to said second source/drain to form a first terminal of said capacitor, said gate forming a second terminal of said capacitor, said [N-well] *a second*

dopant-type well connected to a first power supply, and said substrate connected to a second power supply at a negative voltage with respect to said first power supply;

whereby said capacitor is isolated from electrical noise in said substrate.

In their amendment, Puar and Ranganathan stated that they did not understand why the examiner had rejected Claims 10 and 21-24 as anticipated by Ogoh. According to the inventors, their claims for the graphics controller did not read on Ogoh because Ogoh teaches semiconductor processes and device structures for making a DRAM cell. "Furthermore, if the Examiner is alluding to the fact that claim 21 refers to a capacitor, the applicants do not see what portions of the Ogoh patent are relevant to the language of the claim."

4. ***PTO's Response of April 29, 1996***

On April 29, 1996, the examiner sent the inventors a final action letter allowing Claims 21-24 and 32-50, rejecting Claims 10 and 28 and objecting to Claims 25-27 and 29-31. Claims 10 and 28 were rejected under 35 U.S.C. s. 112 for lack of enablement.FN4 According to the examiner, the inventors did not disclose, to the point of enablement, all possible means of logic and memory. Claims 10 and 28 were further rejected under 35 U.S.C. s. 102 as "being clearly readable on Ogoh or [a] human brain and probably a monkey brain." (strikeout in original). Claims 25-27 and 29-31 were objectionable for depending on a rejected claim, but were otherwise allowable.

FN4. 35 U.S.C. s. 112 provides, in pertinent part:
An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

5. ***Notice of Abandonment***

On December 5, 1996, the examiner sent the inventors a Notice of Abandonment. The examiner stated that the application was abandoned because the inventors had failed to respond to the PTO's final action letter of April 29, 1996.

6. ***Continuation Applications of August 16, 1996***

On August 16, 1996, inventors Puar and Ranganathan filed two continuation applications based on the abandoned application of June 20, 1994. The first application, serial number 698,627, is directed to the invention described in the '955 patent. The second application, serial number 699,090, is directed to the invention described in the '806 patent.

a. ***Application for*** the '955 Patent

The first continuation application is directed to Claims 10 and 28 of the parent application which the examiner rejected for anticipation and lack of enablement.

i. ***Preliminary Amendment of August 16, 1996***

On August 16, 1996, Puar and Ranganathan filed a preliminary amendment concurrently with their continuation application for the '955 patent. The application, as amended, contains two claims. The first claim, an amended version of Claim 10 of the parent application, reads as follows, with the underlining and brackets indicating added and retracted language, respectively:

[10.] *1*. (Preliminarily amended) An integrated circuit *in a semiconductor substrate* comprising

[a logic portion having at least 30K logic gates; and]

a memory portion having a capacity of at least 2 megabits *; and*

at least 30K logic gates with underlying substrate regions, said logic gates interconnected with said memory portion, said logic gates with a voltage supply having a coupling to said underlying substrate regions determined by a voltage of said underlying substrate regions.

The inventors also added a second dependent claim to correspond to Claim 28 of the parent application. The second claim reads as follows:

2. (New) The integrated circuit of claim 1 comprising at least 40K logic gates; and said memory portion has a capacity of at least 7.3 megabits.

In the preliminary amendment, the inventors responded to the examiner's rejection of Claims 10 and 28 for anticipation and lack of enablement. With respect to the Ogoh patent, the inventors stated that while the reference is related to an integrated circuit having more than 2 megabits of memory cells, Ogoh does not teach the use of "at least 30K logic gates," as recited in Claim 10. With respect to the human brain, the inventors stated that they did not understand the correlation between a biological organ and an integrated circuit in a semiconductor substrate. "The applicants understand that the human brain contains a very large number of nerve synapses but do not understand the correlation between a logic gate with underlying substrate regions and a synapse."

ii. ***Notice of Allowance***

On March 18, 1997, the PTO allowed the claims in the continuation application. As approved by the PTO, the '955 patent has an independent Claim 1 and a dependent Claim 2. NeoMagic has asserted both claims against Trident.

b. ***Application for*** the '806 Patent

The second continuation application is directed to Claims 21-27 and 29-50 of the parent application. During the prosecution of the parent application, the examiner had allowed Claims 21-24 and 32-50. The examiner had objected to Claims 25-27 and 29-31 because they depended on a rejected claim, but the examiner stated that the claims were otherwise allowable.

i. ***Preliminary Amendment of August 16, 1996***

On August 16, 1996, Puar and Ranganathan filed a preliminary amendment concurrently with their

continuation application for the '806 patent. The application, as amended, contains twenty-nine new claims which correspond to Claims 21-27 and 29-50 of the parent application.

Claim 1, as submitted in the proposed amendment, reads:

1. (New) An integrated circuit comprising

a logic portion having at least 30K logic gates, said logic gates having first dopant-type and second dopant-type MOS transistors, said first dopant-type MOS transistors having sources connected to a first voltage supply line, said second dopant-type MOS transistors having sources connected to a second voltage supply line, and said second dopant-type MOS transistors placed in a substrate region connected to a third voltage supply line, said third voltage supply different than said second voltage supply; and

a memory portion interconnected with said logic portion, said memory portion having a capacity of at least 2 megabits.

Claim 18 is representative of the other independent claims of the '806 patent. As submitted in the proposed amendment, Claim 18 reads:

18. (New) An integrated circuit comprising

a logic portion having at least 30K logic gates;

a memory portion coupled to said logic portion, said memory portion having a capacity of at least 2 megabits, and

an analog circuit having a capacitor, said capacitor comprising a first dopant-type transistor in a second dopant-type well in a first dopant-type semiconductor substrate, said first dopant-type transistor having a gate, first and second source/drains, said first source/drain connected in common to said second source/drain to form a first terminal of said capacitor, said gate forming a second terminal of said capacitor, said second dopant-type well connected to a first power supply, and said substrate connected to a second power supply at a negative voltage with respect to said first power supply;

whereby said capacitor is isolated from electrical noise in said substrate.

ii. ***Rejection of January 2, 1997***

On January 2, 1997, the examiner rejected all twenty-nine claims in the application for the '806 patent, stating that the claims were indefinite under 35 U.S.C. s. 112. According to the examiner, "the language [of the claims] reads on all memories of at least 30K logic gates and all memories of more than 2 megabits without definitive limits. There is no enabling disclosure for such a range of sizes." The claims were also rejected under 35 U.S.C. s. 102 as being clearly anticipated by Rao, Shimohigashi, or Togei.

iii. ***Response of March 24, 1997***

On March 24, 1997, Puar and Ranganathan submitted a response to the examiner's rejection. The inventors stated that they were puzzled by the examiner's rejection for indefiniteness and anticipation. With respect to indefiniteness, the inventors recited the four independent claims of the application and stated that "[i]t

should readily be evident [that] the language quoted above overcomes the deficiencies which were apparently perceived by the Examiner." With respect to anticipation, the inventors asked the examiner to further elaborate on the reasons for rejecting the claims in light of the prior art.

iv. ***Notice of Allowance***

Rather than elaborating on the reasons for the rejection, on June 13, 1997, the examiner allowed the claims in the application as amended. As approved by the PTO, the '806 patent has twenty-nine claims. NeoMagic has asserted Claims 7, 9, 13, 18, 20, 24 and 26 of the '806 patent against Trident.

II. ***DISCUSSION***

A. ***Claim Construction***

1. ***Basic Principles of Claim Construction***

[1] [2] [3] [4] [5] Claim construction is a matter for the court. *Markman,* 52 F.3d at 979. Claims are construed from the vantage point of a person of ordinary skill in the art at the time of the invention. *Id*. at 986. In construing a claim, a court looks first to the intrinsic evidence of record, namely, the claims, the written description and the prosecution history. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1309 (Fed.Cir.1999). The claim language itself defines the scope of the claim, and "a construing court does not accord the specification, prosecution history and other relevant evidence the same weight as the claims themselves, but consults these sources to give the necessary context to the claim language." Eastman Kodak v. Goodyear Tire & Rubber Co., 114 F.3d 1547, 1552 (Fed.Cir.1997). Extrinsic evidence may be consulted to ensure that the claim construction being considered by the court "is not inconsistent with the clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field." Pitney Bowes, 182 F.3d at 1309.

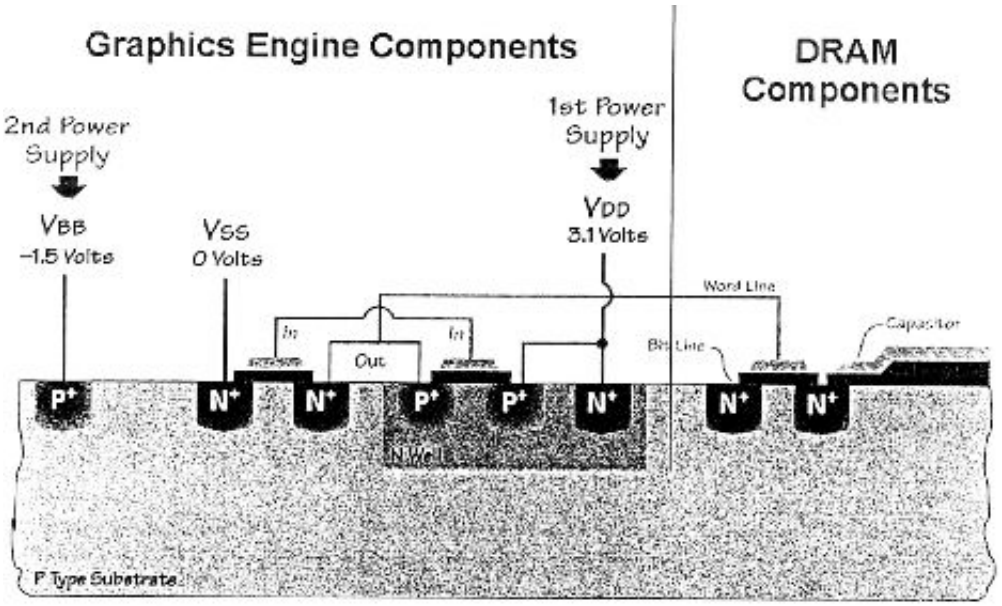
[6] Although the Federal Circuit has held that claims should be read in view of the specification, *see, e.g., id.,* the court has repeatedly cautioned against limiting the scope of a claim to the preferred embodiment or specific examples disclosed in the specification. *See, e.g.,* Ekchian v. Home Depot, Inc., 104 F.3d 1299, 1303 (Fed.Cir.1997); Intervet America, Inc. v. Kee-Vet Laboratories, Inc., 887 F.2d 1050, 1053 (Fed.Cir., 1989) ("[L]imitations appearing in the specification will not be read into claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.' ") (citation omitted).

2. ***Claim Construction for*** the '806 Patent

a. " ***power supply*** **"**

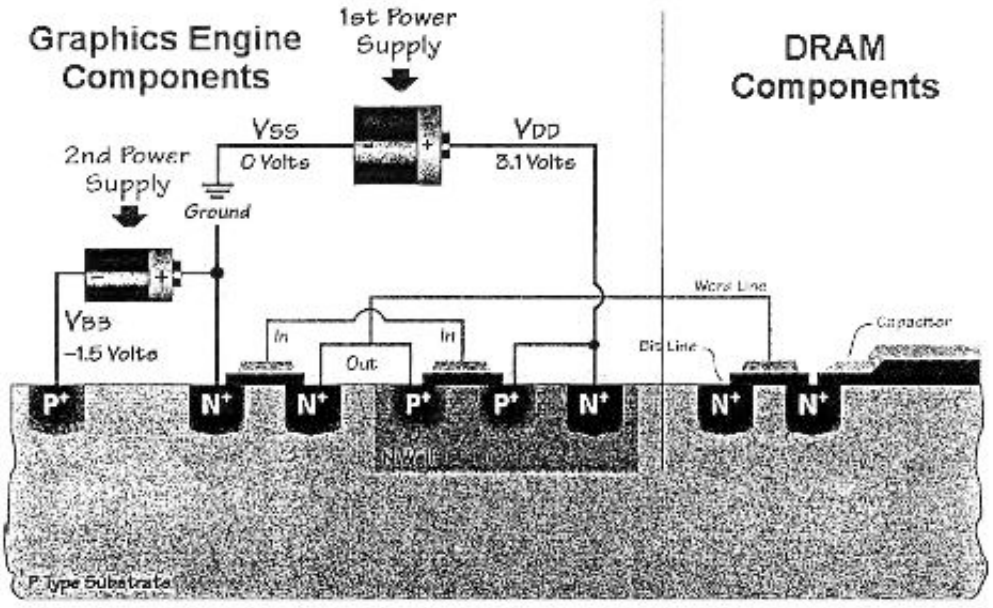
[7] The term "power supply" appears in two of the asserted claims of the '806 patent. Claims 7 and 18 require a "second dopant-type well connected to a first power supply, and said substrate connected to a second power supply at a negative voltage with respect to said first power supply ...." NeoMagic argues that "power supply" means a source connection or line to the integrated circuit that is at a particular voltage. Trident counters that "power supply" requires a complete circuit (with a return path) and cannot consist of a single power supply line.

According to NeoMagic, each of the voltages supplied to the chip, V_{DD}, V_{SS} and V_{BB}, is a "power supply." NeoMagic contends that the "first power supply" referred to in Claims 7 and 18 is the power supply line V_{DD} and the "second power supply" is the power supply line V_{BB}. The following illustration, which was submitted by Trident at the *Markman* trial, helps explain NeoMagic's proposed construction of "power supply." The illustration represents a horizontal cross section of a graphics controller chip with the graphics engine and video memory combined on the same silicon substrate. As before, the N+ and P+ logic gates on the left side of the substrate make up an inverter from a graphics engine. The N+ logic gate and the capacitor on the right side of the substrate are standard DRAM components. V_{SS} and V_{DD} represent source and drain terminals and the voltage applied to the substrate is referred to as V_{BB}.



On the other hand, Trident argues that V_{DD}, V_{SS} and V_{BB} are "power supply lines" rather than "power supplies." According to Trident's proposed construction of "power supply," the term refers to a source of electrical energy, such as a battery, that requires at least two power supply lines to deliver power in an electrical circuit. Thus, Trident contends that "first power supply" refers to the source that delivers electrical energy via the power supply lines V_{DD} and V_{SS}, and "second power supply" refers to the source that delivers electrical energy via the power supply lines V_{SS} and V_{BB}.

The following illustration, which was submitted by Trident at the *Markman* trial, helps explain Trident's proposed construction of "power supply." The illustration represents a horizontal cross section of a graphics controller chip with the graphics engine and video memory combined on the same silicon substrate. The N+ and P+ logic gates on the left side of the substrate make up an inverter from a graphics engine. The N+ logic gate and the capacitor on the right side of the substrate are standard DRAM components. V_{SS} and V_{DD} represent source and drain terminals and the voltage applied to the substrate is referred to as V_{BB}.



i. ***NeoMagic's Proposed Construction***

According to NeoMagic, the claim language, the specification, the prosecution history and the extrinsic evidence support interpreting "power supply" to mean a source connection or line that may be at a particular voltage level.

NeoMagic looks first to the claim language to support its construction. Claims 7 and 18 of the '806 patent specify "a second power supply at a negative voltage with respect to said first power supply." According to NeoMagic, this claim language demonstrates that "power supply" is a source that is "at" a voltage. In addition, NeoMagic argues that Claims 22 and 23, which depend from Claim 18, support its interpretation of "power supply." Claim 22 states that the "second power supply is at approximately -1.5 volts" and Claim 23 states that the "first power supply is at approximately +3.3 volts."

Next, NeoMagic turns to the specification. Although the term "power supply" is not used in the common specification of the '955 and '806 patents, the term "supply voltage" is used in several instances. For example, the specification describes an integrated circuit process that "uses one of the external supply voltages (V_{DD} or V_{SS} depending on the substrate type) as the voltage to bias the substrate." NeoMagic contends that the references to "supply voltage" in the specification "make it clear that ... the supply lines V_{DD}, V_{BB}, and V_{SS} (which indicate voltages supplied to the chip) are examples of 'power supplies' as that term is used in the claims."

NeoMagic also relies on the prosecution history to support its construction of the term "power supply." Specifically, NeoMagic points to several claims in the June 20, 1994 parent application that were later abandoned. For example, Claim 18 of the parent application provided that the "first power supply is at approximately +5 volts, said second power supply at approximately 0 volts and said third power supply at +6 volts." NeoMagic contends that this reference in the prosecution history demonstrates that the inventors

used the term "power supply" to mean any one of the source lines or connections to the various source potentials, V_{DD}, V_{SS} and V_{BB}.

Finally, NeoMagic argues that its construction of "power supply" is consistent with the extrinsic evidence. The McGraw-Hill Dictionary of Electronics and Computer Technology defines "power supply" to mean "a source of electrical energy, such as a battery or power line, employed to furnish the tubes and semiconductor devices of an electronic circuit with the proper electric voltages and currents for their operation." NeoMagic argues that this definition supports its position that a "power supply" is used to provide a voltage potential to the chip. NeoMagic also contends that two prior art patents in the semiconductor field, U.S. Patent Nos. 5,268,597 and 5,030,852, use "power supply" in a manner that is consistent with its construction of the term.

ii. ***Trident's Proposed Construction***

Trident argues that "power supply" means a device which has two or more terminals and which is capable of providing power to a circuit. Trident contends that NeoMagic's proposed construction of "power supply" is contrary to the customary meaning of the term and unsupported by the specification. According to Trident, the use of the term "supply voltage" in the specification does not support NeoMagic's proposed construction of "power supply." Trident argues that all "power supplies" provide "supply voltages" via their power supply lines. Since two power supply lines are required in order for current to flow, Trident contends that one skilled in the art would not refer to a single line connected to a terminal of a power supply to be the power supply itself.

According to Trident, NeoMagic's own expert in electrical engineering, Joseph C. McAlexander, testified during a deposition that "power supply" commonly refers to a complete circuit and not a single power supply line. McAlexander testified that "when you switch something on, you are providing power and providing a source of current and voltage to that one light bulb. And you've got a complete direct circuit, completed circuit. So in that case, I would view that as a single power supply." Trident points to eight patents that use the term "power supply" according to its customary meaning.

Trident also contends that the definition of "power supply" from the McGraw-Hill Dictionary of Electronics and Computer Technology actually supports Trident's construction of the term. According to Trident, the dictionary defines "power supply" as a source of electrical energy, such as a battery or power line, used to furnish the "proper electric voltages and currents ...." Trident notes that the same dictionary defines "power line" as "two or more wires conducting electric power from one location to another." Thus, Trident argues that two power supply lines are required in order for current to flow from a power supply through an electric circuit.

While Trident acknowledges that a patentee can be his own lexicographer, in this case Trident contends that "power supply" has its plain meaning because NeoMagic did not clearly set forth an alternative definition in the specification. Trident argues that NeoMagic's construction of the term is inconsistent with other claims of the invention. According to Trident, the '955 and '806 patents specify that the voltage, V_{BB}, which reverse biases the substrate, is generated from an on-chip charge pump that is separate from the external power supply which provides the voltages V_{DD} and V_{SS}. Therefore, Trident contends that the invention requires two power supplies that share a common ground, V_{SS}.

Trident also argues that the prosecution history does not support NeoMagic's proposed construction of

"power supply." Trident contends that the court should not rely on canceled claims from the parent application to inform its construction of the term. According to Trident, the canceled claim "exists as nothing more than an artifact of a path not taken, and does not come close to providing clear notice of a special definition contrary to common usage."

iii. ***Court's Construction of "power supply"***

The words of a claim should generally be given their customary meaning to one of ordinary skill in the art at the time the patent application is filed. *Markman,* 52 F.3d at 986. The court agrees with Trident that a person of ordinary skill in the art would generally understand the term "power supply" to mean a device which has two or more terminals and which is capable of providing power to a circuit. The McGraw-Hill Dictionary of Electronics and Computer Technology supports this interpretation because it defines "power supply" as a source of electrical energy used to furnish the proper electric voltages and currents. Two power supply lines are required for current to flow from a power supply through an electric circuit. Furthermore, NeoMagic's own expert in electrical engineering testified that "power supply" commonly refers to a source of electrical energy that requires at least two power supply lines.

Nevertheless, the inventors could have intended the term "power supply" to mean something different in the context of their invention. *See* Beachcombers v. WildeWood Creative Products, Inc., 31 F.3d 1154, 1158 (Fed.Cir.1994) (stating that a patentee can be his own lexicographer provided the patentee's definition, to the extent it differs from the conventional definition, is clearly set forth in the specification); Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388 (Fed.Cir.1992) ("Where an inventor chooses to be his own lexicographer and to give terms uncommon meanings, he must set out his uncommon definition in some manner within the patent disclosure."). In Lear Siegler, Inc. v. Aeroquip Corp., 733 F.2d 881, 889 (Fed.Cir.1984), the United States Court of Appeals for the Federal Circuit stated:

So long as the meaning of an expression is made reasonably clear and its use is consistent within a patent disclosure, an inventor is permitted to define the terms of his claims. Nevertheless, the place to do so is in the specification of the inventors application, and the time to do so is prior to that application acquiring its own independent life as a technical disclosure through its issuance as a United States patent. The litigation-induced pronouncements of [the inventor], coming nearly at the end of the term of his patent, have no effect on what the words of that document in fact do convey and have conveyed during its term to the public.

In this case, the inventors did not set forth a definition of "power supply" in the specification or in the prosecution history of the '955 and '806 patents. The term is not even mentioned in the common specification of the patents in suit. NeoMagic argues that the language of canceled claims in the parent application demonstrates that the inventors intended "power supply" to refer to one of the power supply lines, V_{DD}, V_{SS}, or V_{BB}. But the inventors did not define "power supply" in the parent application to have the uncommon meaning proposed by NeoMagic. Furthermore, interpreting power supply as it is commonly understood by one skilled in the art is consistent with the specification of the '955 and '806 patents which requires a second source of electrical energy ("an on-chip charge pump") to reverse-bias the substrate in order to solve the noise problem. Therefore, the court finds, as argued by Trident, that "power supply" refers to a source of electrical energy, such as a battery, that requires at least two power supply lines to deliver power in an electrical circuit.

b. " ***logic gates*** **"**

[8] The term "logic gates" appears in four of the asserted claims of the '806 patent. Claims 7, 13, 18 and 24 of the '806 patent refer to a "logic portion" having at least "30K logic gates" or "40K logic gates." NeoMagic argues that "logic gates" refers to the logic circuitry that makes up the graphics engine and manipulates the video data on a computer screen. Trident counters that the term "logic gates" refers to any kind of logic gate and is not limited to those found in a graphics accelerator.

In order to acquire the proper context to understand claim terms, the court may consult the specification and the prosecution history. *See* Envirco Corp. v. Clestra Cleanroom, Inc., 209 F.3d 1360, 1364 (Fed.Cir.2000); Pitney Bowes, 182 F.3d at 1308-09. In this case, the claims of the '955 and '806 patents are directed to a graphics controller that integrates logic and memory components on a singe semiconductor chip. The inventors use the term "logic gates" consistently throughout the specification to refer to the logic circuitry of the graphics engine. For example, the specification states that "[w]ith the ability to incorporate large amounts of logic and memory in a single integrated circuit, the present invention provides for video memory and logic for graphics control operations in one integrated circuit." Therefore, the court finds, as advocated by NeoMagic, that the term "logic gates" refers to the logic circuitry that makes up the graphics engine and manipulates video data on a computer screen.

c. " *memory portion* "

[9] The term "memory portion" appears in four of the asserted claims of the '806 patent. Claims 7 and 18 of the '806 patent require "a memory portion having a capacity of at least 2 megabits" and Claims 13 and 24 state that "said memory portion has a capacity of at least 7.3 megabits." The parties apparently agree, as does the court, that "memory portion" refers to the circuitry required for a working memory, including the memory cells that store data and the circuitry associated with reading, writing, addressing and refreshing data in the memory cells.

3. *Claim Construction for* the '955 Patent

a. " *voltage supply* "

[10] The term "voltage supply" appears in one of the asserted claims of the '955 patent. Claim 1 of the '955 patent requires "a voltage supply having a coupling to said underlying substrate regions determined by a voltage of said underlying substrate regions." NeoMagic and Trident agree that "power supply" and "voltage supply" are synonymous. Therefore, consistent with its earlier construction of "power supply," the court finds that the term "voltage supply" refers to a source of electrical energy, such as a battery, that requires at least two power supply lines to deliver power in an electrical circuit.

b. " *coupling* "

[11] The term "coupling" appears in one of the asserted claims of the '955 patent. Claim 1 of the '955 patent requires "logic gates with a voltage supply having a coupling to said underlying substrate regions determined by a voltage of said underlying substrate regions." NeoMagic contends that "coupling" means coupled or connected, directly or indirectly. Trident, on the other hand, argues that the term "coupling" requires a voltage potential in the substrate that is different than the voltage potential in the logic gates.

In the specification of the '955 and '806 patents, the inventors describe their method for reverse biasing the substrate to solve the noise problem. According to the specification, the logic circuits are redesigned to decouple the V_{SS} line connected to the source terminals of the N-channel pulldown transistors from the P-

substrate tap. The specification further provides that the logic circuit is connected to a V_{SS} line at 0 volts, while the substrate is tapped by a V_{BB} line at -1.5 volts. By reverse biasing the substrate in this manner, excess charge carriers flow away from the logic and memory portions of the graphics controller.

NeoMagic's proposed construction of "coupling" to mean "connection," is inconsistent with this explanation in the specification.Moreover, NeoMagic's proposed construction of the term is also inconsistent with the claim language. Claim 1 of the '955 patent states that the logic gates have "a voltage supply having a coupling ... determined by a voltage of said underlying substrate." In accordance with the specification, this language requires that the reference potential, V_{SS}, for the logic gates must be different from the voltage potential, V_{BB}, that is applied to the substrate. Otherwise, the phrase "determined by a voltage of said underlying substrate" would be superfluous and meaningless.

Therefore, as advocated by Trident, the court finds that "coupling" requires a voltage potential in the substrate that is different than the voltage potential in the logic gates.

c. " *logic gates* "

The term "logic gates" appears in Claims 1 and 2 of the '955 patent. For the reasons set forth by the court in the discussion of the '806 patent, the court finds that the term "logic gates" refers to the logic circuitry that makes up the graphics engine and manipulates video data on a computer screen.

d. " *memory portion* "

The term "memory portion" appears in Claims 1 and 2 of the '955 patent. For the reasons set forth by the court in the discussion of the '806 patent, the court finds that the term "memory portion" refers to the circuitry required for a working memory, including the memory cells that store data and the circuitry associated with reading, writing, addressing and refreshing data in the memory cells.

III. *CONCLUSION*

For the reasons stated above, the disputed claims of the '955 and '806 patents are construed as follows,

"power supply" refers to a source of electrical energy, such as a battery, that requires at least two power supply lines to deliver power in an electrical circuit;

"logic gates" refers to the logic circuitry that makes up the graphics engine and manipulates video data on a computer screen;

"voltage supply" refers to a source of electrical energy, such as a battery, that requires at least two power supply lines to deliver power in an electrical circuit;

"coupling" requires a voltage potential in the substrate that is different than the voltage potential in the logic gates; and

"memory portion" refers to the circuitry required for a working memory, including the memory cells that store data and the circuitry associated with reading, writing, addressing and refreshing data in the memory cells.

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