

United States District Court,
S.D. New York.

TM PATENTS, L.P and TM Creditors, L.L.C,
Plaintiff.

v.

INTERNATIONAL BUSINESS MACHINES CORPORATION,
Defendant.

No. 97 Civ. 1529(CM)

Nov. 8, 1999.

Owner of patents covering correction of computer errors and massively parallel processing of computer information brought infringement action. The District Court, McMahon, J., (1) held that construction given claims in patent litigation in another district, with different infringer, had collateral estoppel effect in present action, and (2) construed claims.

Claims construed.

In patent claim covering massively parallel processing of computer information, term "message buffer" describing area where messages temporarily wait until transmission could be completed, was not limited to buffer having capacity to store entire message.

Stephen B. Judlowe and Dennis J. Mondolino, Hopgood Calimafde Kalil & Judlowe LLP, New York City, for plaintiffs.

Christopher A. Hughes and Christopher K. Hu, Morgan & Finnegan, New York City, for defendant.

OPINION AND ORDER FOLLOWING *MARKMAN* HEARING

McMAHON, District Judge.

Plaintiffs TM Patents, a Delaware limited partnership formed under the Plan of Reorganization of Thinking Machines Corporation ("Thinking Machines") for the purpose of recovering for infringement of the corporation's patents, and TM Creditors, a Delaware limited liability corporation that represents the interests of the bankrupt's unsecured creditors, are shared successors-in-interest to the patent estate of Thinking Machines, a developer and manufacturer of computers and computer peripheral equipment. Plaintiffs commenced this action against defendant IBM, alleging that certain IBM products infringed three of TM's patents: Patent No. 5,202,979 (the '979 patent); Patent No. 4,899,342 (the '342 patent); and Patent No. 5,212,773 (the '773 patent). The first two patents relate to technologies for storage of data in computers and the detection and correction of errors in such data; the third deals with a strategy for routing

communications in massively parallel processors.

[1] The matter is before the Court for construction of the three patents in suit, as required by *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). After extensive briefing, the parties presented their respective contentions concerning patent construction in light of intrinsic evidence to the Court at a hearing conducted September 8 and 9, 1999. The hearing was attended by, *inter alia*, Professor Jack Lipovski, who had previously been appointed as the Court's disinterested expert and technical advisor. (*See* Order dated July 21, 1999.) The September hearing was limited to issues of intrinsic evidence because, in determining the meaning of the patent claims, the Court must first examine such evidence-including the claims themselves, the specification, and the prosecution history-and determine whether it can derive an unambiguous construction of the claim language from those sources. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed.Cir.1996). As Judge Conner of this Court recently observed, "If this intrinsic evidence permits an unambiguous construction of the claim language, the Court need not, and indeed should not, consider extrinsic evidence, such as testimony from expert witnesses as to special meanings which the terms of the claims have for those skilled in the art." *Evans Medical Ltd. v. American Cyanamid Company*, 11 F.Supp.2d 338, 347 (S.D.N.Y.1998) (citing *Vitronics*, 90 F.3d at 1585), *aff'd*, Nos. 98-1440, 98-1459, 1999 WL 594310 (Fed.Cir. Aug. 9, 1999). Extrinsic evidence should only be relied upon where necessary to resolve an ambiguity in a disputed claim term. *See CVI/Beta Ventures, Inc. v. Tura, L.P.*, 112 F.3d 1146, 1153 (Fed.Cir.1997).

Finding the intrinsic evidence sufficient for *Markman* purposes, the Court construes the patents as set forth below.

A. The '342 Patent

The first patent in suit is a patent for a computer system that has as one of its properties the ability both to detect and to correct errors in data that is stored in the computer. The salient features of the system are its use of an error correction code ("ECC") that has the capacity not just to detect errors in data but to correct them as well, and spare disk drives that "back up" the corrected data, so that there are always two copies in the system.

The disk storage array described in the specifications for the '342 patent consists of 32 dedicated data disks and 7 dedicated ECC disks. In addition, there are 3 spare disks in the array. The disk storage array is connected to a computer by a 64-bit bus, or conductor, along which data is transmitted. The bus is in turn connected to a specialized bus adapter, including an ECC generation circuit, within the array. The bus adapter is thus connected to the disk drive. During transmission of data to the disk array, a 64-bit wide data stream enters the adapter and is split into two 32-bit groups. Each of these 32-bit groups is transmitted to the ECC generation chip to generate a 7-bit ECC. Thereafter, each block of 32 bits and the accompanying ECC bits are sent to all 39 disks in the array through 39 shift registers (computer hardware elements designed to perform shifting of the data contained within them). Data is stored in what is referred to as "bit-stripped mode," meaning that one bit of each of the 32-bit groups of data is stored separately on each of the 32 disk drives.

The 32 data bits and ECC bits are sent together from all 39 disks in the array via the shift registers to a specialized bus adapter, where, using the data and error correction code, the ECC generation circuit chip performs an error detection and correction function on the data bits and delivers the corrected data to the computer. If there is a disk drive failure, the corrected data can be accessed from the spare disk.

The claims in the '342 patent that require construction are Claims 1, 6, 7 and 10.

1. Collateral Estoppel Effects from the EMC Action

TM's suit against IBM is not the first infringement action to reach the stage of a *Markman* hearing in a federal District Court. In 1997, TM also sued a competitor of IBM, EMC Corporation, in a case heard by Chief Judge William G. Young in the United States District Court for the District of Massachusetts. *See TM Patents v. EMC Corp.*, Civil Action No. 98-10206 (D.Mass. Jan. 27, 1999). The case went to trial earlier this year. Immediately prior to the trial, Chief Judge Young held a *Markman* hearing, at which he was asked to construe some, but not all, of the claims disputed in this Court. Judge Young did so, after a two day hearing. IBM asserts that TM is either collaterally or judicially estopped to relitigate the claims that Judge Young construed—with which constructions IBM (a non-party to the EMC action) is in substantial (though not total) agreement. TM argues that Judge Young's rulings, while correct in many respects and perhaps persuasive in others, ought not be accorded former adjudication effect, because the EMC action settled during trial, and because Judge Young's rulings were not sufficiently "final" to be deemed preclusive.

IBM is correct. While this raises an issue of first impression, I conclude that Judge Young's resolution of the meaning of certain disputed patent terms following a *Markman* hearing, at which TM had a full and fair opportunity to litigate the meaning of those terms, is binding on the Plaintiffs in this action.

[2] [3] Collateral estoppel forecloses litigants from contesting matters that were actually litigated and decided in a previous action. *See Blonder-Tongue Lab. Inc. v. University of Illinois Foundation*, 402 U.S. 313, 329, 91 S.Ct. 1434, 28 L.Ed.2d 788 (1971). Four elements must be met for collateral estoppel to apply. First, the issues raised in both proceedings must be identical. Second, the relevant issues must have actually been litigated and decided in the prior proceeding. Third, the party to be estopped must have had a full and fair opportunity to litigate the issues in that prior proceeding. And fourth, resolution of the issues must have been necessary to support a valid and final judgment on the merits. *See Central Hudson Gas & Elec. Corp. v. Empresa Naviera Santa*, 56 F.3d 359, 368 (2d Cir.1995).

[4] The parties before me agree that the first and third of those four elements are met in this case. They disagree, however, as to whether the second and fourth have been satisfied. Since in this particular case, the fourth element (finality) subsumes the second (actually decided), I will address them together.

[5] As to the fourth element, TM notes that the dispute between it and EMC concerning the meaning of certain terms in the '342 patent was never reduced to a final judgment, because the matter was settled before the jury had returned its verdict on the question of infringement. TM adopts the simple and straightforward position that no final, appealable judgment means no finality for collateral estoppel purposes. Unfortunately for TM, that is not the law in this Circuit (or any other, for that matter). Since Judge Friendly's seminal opinion in *Lummus Co. v. Commonwealth Oil Ref. Co.*, 297 F.2d 80, 89 (2d Cir.1961), it has been settled that a judgment that is not "final" in the sense of 28 U.S.C. s. 1291 can nonetheless be considered "final" in the sense of precluding further litigation of issues that were actually determined in such a judgment. Whether a ruling is sufficiently final turns on "such factors as the nature of the decision (i.e., that it was not avowedly tentative), the adequacy of the hearing, and the opportunity for review." *See id.* As Judge Friendly observed, " 'Finality' in the context here relevant may mean little more than that the litigation of a particular issue has reached such a stage that a court sees no really good reason for permitting it to be litigated again." *Id.*; *see also Zdanok v. Glidden Co., Durkee Famous Foods Div.*, 327 F.2d 944, 955 (2d Cir.1964);

Metromedia Co. v. Fugazy, 983 F.2d 350, 366 (2d Cir.1992).

The *Lummus* principle is illustrated by *Georgakis v. Eastern Air Lines, Inc.*, 512 F.Supp. 330 (E.D.N.Y.1981). In *Georgakis*, the plaintiff, who was injured in an airplane crash while traveling with the defendant airline, sought summary judgment on the airline's affirmative defense that the case was covered by the Warsaw Convention, which would have limited the plaintiff's damages to \$75,000. In a prior case arising out of the same crash brought by a different passenger, the court had granted summary judgment against the airline, dismissing the Warsaw Convention defense. The passenger in *Georgakis* invoked collateral estoppel. Rejecting the airline's argument that the interlocutory nature of the earlier decision precluded application of collateral estoppel, the court noted that collateral estoppel "does not require a judgment 'which ends the litigation ... and leaves nothing for the court to do but execute the judgment,' ... but includes many dispositions which, although not final in that sense, have nevertheless been fully litigated." *Id.* at 334 (quoting *Zdanok*, 327 F.2d at 955).

The parties have not called my attention to any case in which a court has applied collateral estoppel to bar relitigation of claims construction issues decided at a prior *Markman* hearing, and I have not located any such decisions. Nonetheless, that proposition seems self-evident.

Markman ushered in a new regime in patent claims construction. Prior to the Federal Circuit's ruling in 1995, disputes concerning the meaning of patent claims were submitted to a jury along with questions about validity and infringement. Thus, until there was a final judgment after a jury verdict, there was no construction of claims, *see, e.g.*, *Tol-O-Matic, Inc. v. Proma Produkt-Und-Marketing Gesellschaft, m.b.H.*, 945 F.2d 1546 (Fed.Cir.1991), and hence, no finality for collateral estoppel purposes. However, after *Markman*, claim construction became a separate legal issue, for determination by the Court. The parties frequently litigate the meaning of those limitations prior to the trial, as occurred in both *EMC* and this case, so that the Court can instruct the jury on the meaning of the patent at the outset of the case. Moreover, the Court limits itself to construing that which is necessary to the resolution of the questions of infringement and validity. The jury is not free to override the Court's construction of the disputed terms. It is hard to see how much more "final" a determination can be.

The facts of the *EMC* case bear out this interpretation. The Massachusetts court was required to construe any disputed terms in the '342 patent for the jury. Prior to the trial in *EMC*, Judge Young held a two day hearing, at which both parties were ably represented-TM by the very same lawyers who represent it in the instant action. The parties identified certain claim limitations on whose meaning they could not agree, and Judge Young heard whatever evidence he thought necessary to interpret those limitations. He then issued a very thorough ruling, disposing of all disputed issues. After ruling, he entertained reargument and made several modifications. He then read his ruling to the jury on the first day of trial, in a preliminary jury instruction. Judge Young used the claim construction to guide his evidentiary rulings. He also gave the jurors copies of what he had read, so that they could refer to his construction during the course of the trial. The jurors were not free to adopt a contrary construction of the patent claims in suit, and they were so advised.

A verdict would not have changed anything about Judge Young's *Markman* rulings. Nothing more remained to be adjudicated; nothing more remained to be decided on the issue of claim construction. The application of the claim to the product was immaterial to the finality of Judge Young's determinations. Thus, under *Lummus* and its progeny, the results of the *Markman* hearing in the *EMC* action were sufficiently "final" to permit application of collateral estoppel-even though the matter to which they were necessary was never reduced to a final judgment after verdict. *See also* Restatement (Second) of Judgments s. 13, comment e

(1980) ("A judgment may be final in a res judicata sense as to part of an action although the litigation continues as to the rest."); *Sherman v. Jacobson*, 247 F.Supp. 261, 268 (S.D.N.Y.1965) (noting that a judgment "may be final as to some matters, even though the litigation continues as to others"). FN1

FN1. Indeed, so final is a *Markman* ruling that one could make a strong case for routinely certifying an interlocutory appeal to the Federal Circuit, pursuant to 28 U.S.C. s. 1292(b), following such determinations. Given the frequency with which the Federal Circuit overrules District Court judges on issues of claim interpretation, such appeals would save millions of dollars and thousands of hours of trial time based on patent constructions that turn out to be erroneous.

It bears noting that one of the Supreme Court's rationales for upholding the Federal circuit's ground-breaking decision in *Markman* was the promotion of uniformity in the meaning to be given to a patent claim. *See Markman*, 517 U.S. at 390-91, 116 S.Ct. 1384. Even prior to *Markman*, the Federal Circuit had held that determination of the scope of a patent claim in a prior infringement action *could* have collateral estoppel effect against the patentee in a subsequent case. *See Pfaff v. Wells Elec. Inc.*, 5 F.3d 514, 517-18 (1993). After *Markman*, with its requirement that the Court construe the patent for the jury as a matter of law, it is inconceivable that a fully-litigated determination after a first *Markman* hearing would not be preclusive in subsequent actions involving the same disputed claims under the same patent. The nature of the *Markman* proceeding is such that finality is its aim.

TM contends that Judge Young's determinations were "avowedly tentative" for several reasons. None is persuasive.

First, Judge Young expressed the view that he was "shaky" about several of his conclusions, and indicated that they were "subject to revision." (Joint Appendix on the Issues of Collateral Estoppel and Claim Construction at A 14-15.) Of course, a Court does not vitiate the collateral estoppel effect of a ruling by expressing some doubt about its conclusions. *See Restatement (Second) of Judgments* s. 13, comment g ("The test of finality ... is whether the conclusion in question is procedurally definite and not whether the court might have had doubts in reaching the decision"); *United States v. McGann*, 951 F.Supp. 372, 380-81 (E.D.N.Y.1997). However, Judge Young made these statements while inviting the parties to move for reconsideration if they disagreed with his constructions (a procedure this Court is not inclined to emulate). The parties accepted his invitation-in particular, TM asked for reconsideration of several issues that all parties believe are key to the question of infringement. Notably, Judge Young ceased to feel "shaky" after further briefing and argument, telling the parties, "You've got the claim construction, you're going to have to live with it." (A 23-23.1.)

Second, TM has cited several passages from the trial transcript in support of its argument that Judge Young had only gone "so far" in construing certain phrases. In particular, TM argues that the Judge had not defined the term "integrated" as used in the phrase "single integrated circuit," (A 42-44), and contends that this constitutes evidence that Judge Young's rulings were not intended to be final. However, at most this omission would mean that Judge Young cannot bind me to a definition of the term "integrated" as used in the phrase "single integrated circuit." It does not mean that his other rulings were avowedly tentative, especially when both his words and his behavior during the trial are to the contrary.

Plaintiffs next argue that the *Markman* constructions were never reviewed by a higher Court-a not insignificant proposition when nearly 40 percent of claims constructions are changed or overturned by the

Federal Circuit. *See* *Cybor Corp. v. FAS Technologies., Inc.*, 138 F.3d 1448, 1476 (Fed.Cir.1998) (Rader, J., dissenting). However, the only reason Judge Young's conclusions were not reviewed on appeal is that the case was settled. A party who cuts off his right to review by settling a disputed matter cannot complain that the question was never reviewed on appeal. The *Markman* rulings were not vacated as part of the settlement. They therefore remain preclusive. *See* *Hartley v. Mentor Corp.*, 869 F.2d 1469, 1472-73 (Fed.Cir.1989); *Wellons, Inc. v. T.E. Ibberson Co.*, 869 F.2d 1166, 1169 (8th Cir.1989); *Siemens Med. Sys., Inc. v. Nuclear Cardiology Sys., Inc.* 945 F.Supp. 1421, 1436 (D.Colo.1996); *Ossman v. Diana Corp.*, 825 F.Supp. 870, 878 (D.Minn.1993). FN2

FN2. Although these rulings involved post-verdict settlements reached prior to appeal, rather than settlements reached before judgment, they are still applicable to this case. Judge Young's rulings are preclusive, not because they were made before the jury returned a verdict, but because of the special finality of a *Markman* ruling in a patent case.

Fourth, TM argues that a *Markman* adjudication cannot be preclusive prior to verdict because there is no requirement that a Court construe the claims in suit prior to giving its final instruction to the jury. Indeed, it appears to be the practice in at least one federal district court to hold the *Markman* hearing during the trial, with the Court issuing its ruling when it instructs the jury at the close of the case. *See, e.g.*, *Johns Hopkins Univ. v. Cellpro*, 894 F.Supp. 819, 826 (D.Del.1995). Of course, if Judge Young had followed such a procedure, then there would be no issue preclusion from the *EMC* case. But he did not. He held a two day hearing, following which he issued a ruling construing the claims. He then heard reargument and fine-tuned his ruling, telling the parties to "live with it." He read the ruling to the jury and handed each juror a copy. The fact that he could have done otherwise does not vitiate the preclusive effects of what he actually did. Had Judge Young followed the Delaware procedure and announced his *Markman* ruling at the close of the evidence, only to see the case settle while the jury was deliberating, I have no doubt that his views about the meaning of the disputed claims would be just as preclusive as if they had been announced prior to trial. The fact that the judge makes the ruling is sufficient under *Lummus*; when he does so is irrelevant.

The cases TM cites for the proposition that the collateral estoppel effects from claim construction should be narrowly limited to matters that were essential to a judgment (of validity or infringement)-cases such as *Jackson Jordan, Inc. v. Plasser Amer. Corp.*, 747 F.2d 1567 (Fed.Cir.1984); *A.B. Dick Co. v. Burroughs Corp.*, 713 F.2d 700 (Fed.Cir.1983); and *Studiengesellschaft Kohle v. Eastman Kodak Co.*, 616 F.2d 1315 (5th Cir.1980)-are inapplicable in the post- *Markman* era, at least when the district court holds a special pre-trial hearing, as Chief Judge Young did in the *EMC* case. These authorities were decided at a time when patent claims were construed during jury deliberations. It therefore made perfect sense to limit the collateral estoppel effects emanating from a jury's judgment on issues of validity and infringement to matters of claim construction that were necessarily comprehended in the verdict. That rule makes no sense when a court, acting as a matter of law, draws binding conclusions about the meaning of disputed patent terms for the benefits of the litigants and the jurors. Even the one post- *Markman* case cited by TM for this proposition, *Phonometrics, Inc. v. Northern Telecom, Inc.*, 133 F.3d 1459 (Fed.Cir.1998), is not inconsistent with the principle adopted by this Court. Although the *Phonometrics* case was decided after *Markman*, it followed an earlier decision that was not given preclusive effect and was decided several years before *Markman*. *See* *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384 (Fed.Cir.1992).

Finally, TM argues that a recent Federal Circuit case, *Odetics, Inc. v. Storage Tech. Corp.*, 185 F.3d 1259 (Fed.Cir.1999), worked a change in the law and demonstrated that some of Judge Young's rulings were

erroneous. To that extent, TM contends, collateral estoppel ought not be applied, since it would be clear error to give preclusive effect to a ruling that was entered prior to "a significant change in the legal atmosphere." *Bingaman v. Department of the Treasury*, 127 F.3d 1431, 1437-38 (Fed.Cir.1997), citing *Commissioner v. Sunnen*, 333 U.S. 591, 600, 68 S.Ct. 715, 92 L.Ed. 898 (1948).

TM is correct about the legal principle, but incorrect when it asserts that *Odetics* worked a change in the law. The *Odetics* opinion cited above was the eighth and most recent in the protracted *Odetics* litigation. In that decision, the Federal Circuit did not address the issue of claim construction, as TM asserts, but rather reviewed the trial court's infringement decision, notably, its comparison of the accused product with the previously construed patent claim (construed under the means-plus-function limitation). The claim limitation was construed in an earlier decision, *Odetics, Inc. v. Storage Tech. Corp.*, 1997 WL 357598 (Fed.Cir. Jun. 25, 1997). Thus, the recent *Odetics* ruling did not work any change in the law with respect to that issue, although the decision will prove relevant to some of the issues of construction on claims that are not subject to collateral estoppel.

If "finality" in the collateral estoppel context "mean[s] little more than that the litigation of a particular issue has reached such a stage that the court sees no really good reason for permitting it to be litigated again," *Lummus*, 297 F.2d at 89, I see no reason to permit TM a second chance to litigate the meaning of the claims previously construed by Judge Young. Therefore, I hold that collateral estoppel forecloses TM from relitigating the meaning of limitations (ii), (iii), (vii) and (viii) of Claim 1, and the corresponding limitations (i), (iii) and (iv) of Claim 7, *see infra* at part 2(c). The other claims in dispute before me were not disputed in Massachusetts, and TM is free to argue for any interpretation of those limitations here. And, of course, IBM is not precluded from litigating anything at all. So there is plenty for this Court to decide from scratch.

Finally, I have to observe that this issue of collateral estoppel, which has taken on a life of its own in this action (no doubt due to my preoccupation with it), is of marginal practical importance, because I agree with just about everything Judge Young did when he construed the claims in the EMC action. Nonetheless, I have no doubt that collateral estoppel would apply against TM on the previously litigated claims even if I thought everything Judge Young decided was wrong. This does not, however, mean that I agree with all the "gloss" that IBM puts on certain key rulings by Judge Young, a point which I discuss further below.

IBM has relied upon two other issue preclusion theories, judicial estoppel and party admissions under Fed.R.Evid. 801(d). It is not necessary for me to reach those arguments, although I do note that IBM's invocation of judicial estoppel is improper, as that doctrine applies only to inconsistent factual positions, not to issues of law. *See Bates v. Long Island RR Co.*, 997 F.2d 1028, 1037 (2d Cir.1993); *TLC Beatrice Int'l Holdings, Inc. v. CIGNA Ins. Co.*, 1999 WL 33454 at (S.D.N.Y. Jan.27, 1999).

2. Construction of the Disputed Claims in the '342 Patent

Before going to the individual disputed claims, I observe that the '342 patent does not seem to me a particularly difficult patent to construe. For the most part, the words are clear and unambiguous and can be given their plain meaning. My reading of Judge Young's decision is that he did precisely that, and I have no fundamental disagreement with any of his conclusions.

Most of what IBM asks me to overlay onto Judge Young's prior construction of Claim 1 (which is where the disputed issues arise) derives from the patent specification. IBM takes the position that the only invention disclosed in the patent application was the preferred embodiment, in all its detail. However, IBM

overlooks settled rules of patent construction that are discussed below. Absent an indication that the plain terms of the patent were not intended to control, I decline to follow IBM's suggested approach to interpretation of the claims.

(a) Claim No. 1 (Independent Claim): Disputed Limitations

(i) 1. A multi-unit memory system comprising:

[6] This claim, which was not disputed before Judge Young, means precisely what the words say. "A multi-unit memory system" is "a" (that is to say, one, or a single) system that uses two or more data storage memory units. Of course, the fact that the patent claims "a" system does not mean that IBM or some other party would escape liability for infringement by constructing two or three or even more such multi-unit memory systems and somehow linking them together or causing them to operate together.

[7] [8] There is no reason to read anything further into the very simple words used by the claimant. There is no mention of a "single array" in the patent claim, and I decline to adopt IBM's suggestion that I read such a limitation into the claim, applying the settled principle of patent construction that the language of the claim defines its scope, *see* Mantech Environmental Corp. v. Hudson Environmental Servs., Inc., 152 F.3d 1368, 1373 (Fed.Cir.1998), and that the words of a claim are to be construed in accordance with their ordinary meaning to persons in the relevant field of technology, unless it appears that the inventor used them otherwise. *See* Bell Communications Research, Inc., v. Vitalink Communications Corp., 55 F.3d 615, 620 (Fed.Cir.1995). In particular, claims are not to be limited or construed by reading in extraneous words from written descriptions or specifications that are not contained in the claims themselves. *See* Laitram Corp. v. NEC Corp., 163 F.3d 1342, 1347 (Fed.Cir.1998). This rule is not inconsistent with the principle that claims should be construed in light of the patent specification, *see, e.g.*, Bell Communications, 55 F.3d at 620, but simply recognizes that the claims of a patent are not limited to the preferred embodiment that is described in the specifications. *See* Ekchian v. Home Depot, Inc., 104 F.3d 1299, 1303 (Fed.Cir.1997).

Throughout this proceeding, IBM has contorted the plain meaning of words and phrases used in the patent claims themselves by referring to the written description, including the specifications and the embodiment disclosed therein. In construing this patent (and, indeed, all three patents), I have adopted the principle that, where the language of the claim is clear and unambiguous, I will read nothing additional into it. If this means that the patent turns out to be invalid (which is a decision for the jury, not for the Court), then so be it. Although courts are to construe claims so as to sustain a patent's validity where possible, *see* ACS Hosp. Systems, Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577 (Fed.Cir.1984), courts are nonetheless bound to follow the other rules of construction discussed above. *See id.*

(ii) ... an error correction code generation circuit which generates for each block of data to be stored in said memory system an error correction code, ...

(iii) ... each block of data comprising a first plurality of digits and each error correcting code comprising a second plurality of digits from which at least one digit of error may be detected and corrected in the block of data ...

[9] [10] This is the first claim that is affected by collateral estoppel from Judge Young's decision. In the *EMC* case, Judge Young construed this claim language as follows: "[Error correction code generation circuit] means a single integrated circuit which generates the claimed error correction code ... Data, as I have already said, is information. Here, the data is in the form of digits. A block of data, as used in this

phrase, means a group of data bits which may be corrected by another group of bits called error correction bits. The data is information to be stored in the computer." (A 17.)

This construction, relying as it does on the plain meaning of the words used in the claims limitation, is plainly correct. The only arguably unclear term used by Judge Young is his definition for the phrase "error correction code circuit," which he defined as a "single integrated circuit which generated the claimed error correction code." (A 17.) The words "single integrated circuit" do not appear in the claim, and TM urges that Judge Young erred in so limiting its claim.

Putting to one side the fact that TM is collaterally estopped to challenge Judge Young's ruling, TM is simply incorrect. The limitation refers to "an"-i.e., one-error correction code circuit. In other words, the literal language of the claim calls for one circuit that generates an error correction code. The patent specification discloses that this circuit was a single integrated circuit-that is, "... an interconnected array of active and passive elements integrated with a single semiconductor substrate or deposited on the substrate by a continuous series of compatible processes, and capable of performing at least one complete electronic circuit function." *McGraw Hill Dictionary of Scientific and Technical Terms* (3d. ed.1984). Judge Young did not err when he restricted the claim in limitation (ii) to error correction code circuits that generated the correcting digit via a single integrated circuit.

That said, I can think of ways to phrase parts of the interpretation that might be easier for a jury to understand, and I do not understand the doctrine of collateral estoppel to require me to quote Judge Young verbatim. I will, therefore, rephrase it as follows:

The multi-unit memory system I have just described contains a single integrated circuit that is called the error correction code circuit. What does this circuit do? It generates-that is, it creates-something called an error correction code, which is a group of mathematically interrelated bits. It creates one of these error correction codes for each block of data that is to be stored in the memory system.

Now, let's take a look at what some of those words mean-the words that might be unfamiliar to you. Data is simply information. In a computer, data is stored as digits-specifically, as the digits 0 and 1, as will be explained to you during the course of the trial. Each individual digit is known as a bit, which is a contraction of the phrase "binary digit." For those of you who remember the binary number system from your high school math class-that's also known as the Base 2 system-0 and 1 are the two digits in the binary system. So a block of data is two or more data bits that are used to code information in a computer. That's what the phrase "plurality of digits" means-it's just a fancy way of saying more than one digit.

An error correction code is also a plurality of digits-remember, that means more than one of those binary digits, 0 and 1-and the error correction code has a particular purpose, which is to detect and correct an error in a block of data. So for every block of data in our multi-unit memory system, there is an associated error correction code, which is capable of doing two things: determining that at least one of the bits in the associated data block is correct, and correcting the error that it has detected, by generating a new, corrected bit of data.

IBM, relying on the specification, has urged me to insert a further limitation: namely, that any block of data can contain no more than 32 bits. However, there is no reason to read any such requirement into the claim, since there is nothing about the phrase "block of data" that necessarily suggests the size of the block-as opposed to the phrase "an error code generation circuit"-which does suggest a single circuit rather than

multiple circuits. Of course, it is possible that a jury would not find infringement of the Plaintiff's claims by a system that can detect and correct errors in larger blocks of data, but that does not bear on the construction of the claim.

(iv) ... a plurality of read/write memory units, which store the digits of said blocks of data and associated error correction codes generated by said error correction code generation circuit and read said digits ...

(v) ... at least some of the different digits of each code and its associated data block being stored in different memory units.

[11] Again, these words are not difficult to interpret in light of their plain meaning. These limitations require that there be more than one memory unit to store the blocks of data and their associated error correction codes. These units must be what are known as read/write units—that is, they must be able to store the data bits and to read them. Moreover, at least some of the different digits of each code and its associated data block must be stored in different memory units. That is, if we have a data block reading 100101001, and an error correction code that corresponds to that particular data block, at least some of the digits of the data block must be stored in a different memory unit from the error correction code.

[12] IBM argues strenuously that no portion of the error correction code can reside in the same memory unit where the underlying block of data is found, relying on the specifications and the preferred embodiment, which clearly show 32 memory units storing only data and 7 associated memory units storing only error correction codes. The claim limitation as written, however, encompasses more than the configuration urged by IBM. This conclusion is reinforced by looking at unasserted Claim 5, which depends on Claim 1 and which clearly states that the *all* the error correction code bits must be stored on separate memory units from the data block digits. Under the rule of claims differentiation, when some claims are broad and other, dependent claims are explicitly narrower, the limitation of the narrower claim cannot be read into the broader claim, even to avoid invalidity or to escape infringement. *See* Karlin Technology Inc. v. Surgical Dynamics, Inc., 177 F.3d 968, 971-72 (Fed.Cir.1999); Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1054-55 (Fed.Cir.1988); D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1574 (Fed.Cir.1985). IBM is free to argue at trial that the patent as construed is invalid, but I am not free to overlook the doctrine of claim differentiation in order to construe the claim limitations more narrowly than they are written.

Similarly, I reject IBM's effort to have me rule that claim limitation (iv) requires that the block of data and its associated error correction code be stored across all of the memory units in the array. Again, IBM is trying to convince me that the claim should be construed so as to limit the invention to its preferred embodiment as described in the specifications. I decline to do so.

(vi) ... at least one spare read/write memory unit that is similar in operation to an individual read/write memory unit of said plurality of read/write memory units ...

[13] Once again, the plain meaning of the words used in the limitation dictates the construction to be given by this Court. The phrase "at least one" does not, as IBM urges, mean "one and no more than one." Rather, as TM notes, it means "one or more than one." Therefore, the claim limitation teaches that the multi-unit memory system should have one or more than one "spare" memory unit, with "spare" used in its ordinary dictionary sense (a la "spare tire").

(vii) ... means for generating from the digits of a block of data and associated error correction code read from said memory units a digit which corrects an error in a digit read from one of said memory units, said generating means operating on a sequence of said blocks of data and associated error correction codes to generate a sequence of correct digits, and

(viii) ... means for accessing the spare read/write memory unit to store therein said sequence of correct digits as the sequence of correct digits as the sequence of blocks of data and associated error correction codes are read from the plurality of read/write memory units.

[14] [15] These two claims must be interpreted in accordance with the dictates of 35 U.S.C. s. 112(6), which was inserted into the patent laws after the United States Supreme Court invalidated so-called "means-plus-function" claims limitations. *See Halliburton Oil Well Cementing Co. v. Walker*, 329 U.S. 1, 67 S.Ct. 6, 91 L.Ed. 3 (1946). Recitations that are properly considered to fall within this rule are construed differently than other limitations, in that any infringing device or process must both perform the identical function as does the claimed invention and must do so with a structure that is identical or equivalent to that described in the specification. *See Odetics*, supra, 185 F.3d 1259, 1999 WL 455530 at *4. Thus, unlike an ordinary limitation, a means-plus-function limitation is to have the specification read into it. That is precisely what Judge Young did when he construed the above limitations in the EMC litigation. I find no fault with his conclusions-though I do not read them in quite the same way that IBM does.

Judge Young construed limitation (vii) as follows:

[E]ach means claim requires the description of a function, and then an associated structure to accomplish that function. Here the claimed function is to generate a corrected bit by reading all of the bits of a block of data and its associated error correction code, including any erroneous bit. The disclosed structure of this claim is a Texas Instrument semiconductor chip, or its structural equivalent, which generates a corrected digit using a Hamming code, or its structural equivalent. (A 18.)

Both parties seek changes in Judge Young's reading. TM is, of course, collaterally estopped from challenging Judge Young's conclusions, but IBM is not. However, the language IBM proposes to add to Judge Young's reading of the patent is unsupported.

IBM asks this Court to rule that structural equivalent of the Texas Instruments 74AS632 integrated circuit chip is any other integrated circuit chip for generating a Hamming code. The Hamming code is a particular form of error correction code, which both detects and corrects errors by recalculating stored data to match the data when read by the computer. IBM-which uses a different sort of error correction method, known as simple parity, in the alleged infringing products (known as the RAID 3, 4, 5 and 6 systems FN3), insists that any system that detects and corrects data by using any other error correction code necessarily falls outside the ambit of the claimed invention.

FN3. The Hamming code system contained in the specifications for the '342 patent is a RAID 2 system.

IBM's effort to win the battle of infringement at the *Markman* stage is predictable, but this Court has no intention of usurping the jury's function. Since even a means-plus-function claim can be infringed by the structural equivalent of a disclosed embodiment, it would be error for me to interpret the claim as being limited to systems that employ Hamming code to detect and correct errors-particularly since a Court is not

to construe patent claims with an eye to the product at the *Markman* phase. See *CVI/Beta Ventures*, 112 F.3d at 1153. It may be, as IBM urges, that there is no structural equivalent to the Hamming code, and that its RAID 3, 4, 5 and 6 systems do not infringe the patents in this case because they perform the identical function but in a fundamentally different way. That, however, is a question of equivalence. It is not before this Court today.

Moreover, IBM's insistence that such details as Hamming code and Texas Instrument chips are literally part of what the inventor under the '342 patent is claiming, while understandable, is unwarranted. Here, the recent *Odetics* case is instructive. In that case, the district court ruled that the individual components of an overall structure that corresponded to a claimed function-in that case, a "rotary means" for accessing stored videocassettes-were part of the claim limitation. Although, as IBM notes, the issue of claim construction was not directly before the court, the Federal Circuit reversed, stating:

The claim limitation is the overall structure corresponding to the claimed function. That is why structures with different numbers of parts may still be equivalent under Section 112, para. 6, thereby meeting the claim limitation. The appropriate degree of specificity is provided by the statute itself; the relevant structure is that which "corresponds" to the claimed function. Further deconstruction or parsing is incorrect. *Odetics*, 1999 WL 455530 at *6.

Judge Young was quite careful to rule that structural equivalents of the TI semiconductor chip (i.e., single integrated circuits) and structural equivalents of the Hamming code (which he found to be "other codes FN4 that perform precisely the same function, which were known at the time of this patent") fell within the scope of the claimed invention. Try as it might, IBM cannot convince me to read the word "equivalents" out of the claim construction. I adopt Judge Young's construction of limitation (vii).

FN4. The question of what constitutes a "code" that performs the same function as a Hamming code is critical to the equivalence portion of the case. It turns on whether the term "parity" can be construed as in all significant respects identical to "error correction *code*," as TM argues, or whether there is a fundamental structural difference between an error correction *code* -even one that employs a parity calculation, as Hamming does-and the concept of parity itself. This is a question that the jury will confront at the infringement trial.

[16] The only disputed portion of limitation (viii), the "means for accessing" claim, is Judge Young's description of the disclosed structure. Otherwise, both parties are agreed that this limitation requires the ability to access the "spare" memory/memories for the purpose of storing a "back-up" set of corrected digits at the same time that the corrections are being sent to the main memory/memories. I can see no reason for adding IBM's proposed language to Judge Young's carefully crafted description of the disclosed structure-"a set of multiplexers, shift registers, and control signals that direct a corrected bit to the spare disk drive or its equivalent ..."-and I decline to do so. IBM's proposal to have a claim construction that "fixes the location of the spare memory unit in the single array of memory units" is grounded, like so many of its arguments, in its desire to have the Court limit the claims to the details of the specification-an approach that I have rejected. IBM's proposal also runs afoul of my decision that the phrase "at least one spare memory unit" is not restricted to the singular.

(b) Claim 6 (Dependent Claim): Disputed Limitations

There are no disputed limitations in Claim 6, a claim that further limits the scope of Claim 1 by adding the requirement that the read/write memory units (main and spare) consist of "identical" disk drives. This limitation describes the preferred embodiment. (A 279.)

(c) Claim 7 (Independent Claim): Disputed Limitations

Claim 1 covers a computer system. Claim 7 relates to a method for performing the functions that are performed, *inter alia*, by the computer system described in Claim 1. Both parties agree that the limitations of independent claim 7 should be construed in the same manner as their counterpart limitations in independent claim 1, because the claims are analogues. *Southwall Technologies, Inc. v. Cardinal IG Co.*, 54 F.3d 1570 (Fed.Cir.1995). I accept their invitation to construe the corresponding limitations in the two claims identically.

(d) Claim 10 (Dependent Claim): Disputed Limitations

As was true of claim 6, there are no disputed limitations in dependent claim 10.

B. The '979 Patent

The specifications for the '979 patent, like those for the '342 patent, show a data storage system consisting of 39 disk drives, including 32 disks for storing data and seven disks for storing error correction code. The principal difference between the two patents is that the '979 patent does not include the use of a spare memory unit to back up the main memory units.FN5

FN5. The '979 application actually preceded the '342 application and describes a more primitive error detection and correction system.

The only disputed claim is Claim 13.

1. Construction of Disputed Claims

(a) Claim 13 (Independent claim: Disputed Limitations)

(i) A system for storing digital data words, each data word having a plurality of multi-bit data portions, and for storing said data words in response to a storage request received over a parallel data bus said system comprising ...

[17] The key disputed term in this part of the definition is "data word." TM contends, without any particular intrinsic evidence to back its contention, that "data word" is no different than "data block" in the '342 patent. The question that arises is why the inventor would use a different phrase to convey the same concept. The issue becomes more acute because the term "word" has a specific and particular meaning in computerese. It is a term of computer architecture, referring to the amount of data that can be transferred to or from input or output devices in one memory cycle. *See S. Handel, A Dictionary of Electronics* 392 (2d Ed.1966). The term "block of data," as I have interpreted it in connection with the '342 patent, contains no such specialized meaning and no such restriction. Therefore, I am unpersuaded that the two terms should be construed interchangeably.

IBM would have me construe "data word" even more narrowly, as encompassing only groups of bits that

are "small multiples of 32 bits," on the ground that the largest "word" shown in the patent specifications is 256 bits, or 8 times 32 bits. IBM offers no persuasive reason why I should insert this limitation into the term "word," although its counsel-while agreeing at oral argument that a "word" is indeed the amount of data that can be transferred in one memory cycle-suggested (without evidentiary support) that only a small amount of data could be transferred in a single memory cycle using current technology. This may or may not be true, but it is not necessary to interpolate so precise a limitation into the patent claim.

Of course, I must interpret this limitation in light of the next following limitation, which specifically states that each data storage unit shall store "a respective one" of the several multi-bit data portions for each data word. (See below, page 32.) Thus, to fall within the literal patent claim, there must be an equivalent number of multi-bit data word portions and data storage units. That does not, however, mean that there may only be 32 data portions and corresponding 32 storage units in order to fall within the limitation. It is not inconceivable that a system could contain several hundred, or even thousand, data storage units, which would therefore be capable of storing a corresponding number of multi-bit word portions in parallel, one data portion to a memory unit.

IBM would also have me declare that the bits of data within the word must be logically related in the sense that they are part of the same unit of information sent from the computer, and will be part of the same unit of information when returned to the computer. To illustrate its point: IBM contends that "Mary had a little lamb" could be a data word, because all the "bits" (that is to say, all the letters) are logically related; but "Mary had a little lamb and the Yankees are World Champions" could not, because this statement contains two ideas that are not logically related. TM argues that there is no such limitation in the patent claim, and points out that imposing any such limitation would exclude the preferred embodiment from the scope of the patent-a highly disfavored way of construing a patent, one that is "rarely, if ever, correct." *See Vitronics*, 90 F.3d at 1583. TM is correct, and I decline to impose this restrictive definition on the claim.

The parties agree that the term "parallel data bus" means a system containing more than one conductor within a computer along which information is transmitted from a source within the computer to a destination within that computer. And the term "multi-bit data portions" necessarily means data word subsets of two or more bits, because a system described in prior art could read only one bit at a time. (A 605.)

I will thus describe this first limitation for the jury in the following terms:

We are dealing in this '979 patent with a system for storing something called digital data words. Digital means comprised or made up of digits, which as we already know can be either 0 or 1. And data, as we already know, means information-in this case, information that is encoded into digital form. Now exactly what is a data "word?" Well, the term "word," in computerese, means the amount of data, or the number of bits (binary digits, or 0s and 1s), that can be transferred to or from input/output devices in a single memory cycle. It is not a specific number of bits; rather, it is whatever number of bits can be transferred to or from input/output devices in one memory cycle. We will hear a lot more about input and output devices and memory cycles as the trial wears on.

In this particular system discussed in the '979 patent, each digital data word is made up of two or more sub-parts, and each of those sub-parts contains more than one bit, that is, two or more bits. For example, if you had a data word that was 64 bits long, it might have 8 multi-bit data portions consisting of 8 bits each. Or it might have 32 multi-bit data portions consisting of 2 bits each. But however these sub-parts, these data

portions, get whacked up, each one must have at least 2 bits.

Now our system, to be comprehended within the '979 patent, must have the capacity to store the data words in a particular way. The system has to be able to store the data words in response to a storage request that is received over something called a parallel data bus. When you think about a data bus, I want you to think about a Bee Line bus, or a city transit bus, or a school bus. Those are devices for transporting people from one place to another. Well, in a computer, a bus is a device for transporting data from one place to another. It consists of one or more conductors, along which information is transmitted from a source to a destination. And a parallel data bus is more or less exactly what it says: it is a data bus that has multiple conductors, or more than one wire, if you prefer, which can transmit data at the same time-in parallel, so to speak-from one place within a disk system to another.

(ii) ... a plurality of data storage units each having a mechanically driven medium, said media of said different storage units being driven independently of each other, said data storage units storing data words with each data storage unit storing in parallel a respective one of said multi-bit data portions for each data word, each data storage unit including an arrangement for writing data portions onto its respective storage media ...

[18] This limitation deals with "data striping," which is the salient storage feature of the '979 patent. Data striping refers to a process of storing portions of a single unit of data (in this case, the previously defined "data word") in multiple memory units. Striped data is literally spread out over several different storage media, so that all those media must be accessed in order to obtain the entire data unit. To offer a simple example: if the word "cat" were split into its three component parts, and each part were stored in a different memory unit, the word would be striped. This particular limitation calls for striping data so that each data storage unit in the system stores in parallel one multi-bit data portion of each data word. Thus, as noted above, the patent claim contemplates that there will be an equivalent number of data storage units and multi-bit data portions within a data word.

The units in this limitation are specifically referred to as "data storage units." IBM argues, as it did in connection with the '342 patent, that, to fall within the patent, these storage units may store only data and may not contain error correction code. As was true with the '342 patent, TM disagrees.

I find that I must reach a different conclusion with the '979 patent than I did with the '342 patent on this particular point, because there are two significant differences between the two sets of claims. First and foremost, the plain language of the '979 claim is not the same as the language of the '342 claim. The '979 language identifies two types of storage units: "data storage units" (this limitation) and "correction bit storage units" (the next limitation). Second, confirming that the inventor intended the plain meaning of the words he used in drafting the claim, there are no fewer than five prior art distinctions in the patent on the ground that the disks in the '979 invention are dedicated either to data or to memory, while the disks in prior art were not so dedicated. To take one example, in a Preliminary Amendment following the rejection of its original claims, the patentee distinguished a prior art reference in an article by Professors Haran Boral and David J. DeWitt, entitled *Database Machines: An Idea Whose Time Has Passed?* (A 725), by noting that the article did "not suggest providing a separate error correction storage device ..." (A 670.) In another submission, TM advised the Patent Examiner that "One general feature of applicants' invention (recited in claim 1) is in storing a data word on one mechanically driven medium (i.e., a disk drive) *and storing one or more error correction bits for the data word independently on a medium that is mechanically driven independently from the medium on which the data word is stored (e.g., on a separate disk drive) ...*"

(emphasis added). (A 440.)

Finally, the parties disagree about the meaning of the term "storing in parallel" as used in this particular limitation. IBM contends that a necessary construction of the patent is that none of the data storage units can operate independently of the others; they must all be accessed simultaneously (synchronously), in a single operation, in order to store the data word. In support of its argument, IBM points out that, at column five, lines 24-28 of the patent, the inventor writes, "The storage and retrieval of data via all of the SCSI buses to the controllers occurs synchronously in parallel. That is, from the point of view of the bus adaptor, related data is passed in a single operation over all of the SCSI buses at the same time."

TM argues that the phrase "storing in parallel" should be read literally, as applying only to storage, which TM concedes must be across multiple storage media. It urges that this phrase neither literally says nor fairly implies anything about how data are retrieved and contends that data may be accessed asynchronously as well as synchronously within the literal terms of the patent. TM also points out that Thinking Machines's response to the Patent Examiner distinguished a prior art reference to the Boral article on the basis that the article (unlike TM's application) did not permit "data transfer which may be asynchronous." (A 608.)

The phrase "storing in parallel" is discussed extensively in the file history, primarily by way of differentiating the '979 patent from other inventions of the time. It appears that the Examiner allowed the claims as proposed because of the addition of the words "in parallel" to the claim in question. Construction of this term, then, would appear to be key to this invention. I find it to be the most difficult question of all those presented to me, precisely because the file wrapper contains references that can be read to support either point of view.

The Court's expert, Professor Lipovski, has written a letter that affords valuable assistance in this regard. Professor Lipovski notes that the SCSI protocol-which is described in the patent (and therefore constitutes intrinsic evidence), and which all parties agree is pertinent to the reading and writing of data under this patent-does not have a command to synchronize multiple disks so as to read or write data in parallel (i.e., at exactly the same time). It does, however, have commands that can be sent to multiple disks so that data can be sent to or from the disks on which they are stored using a common clock (i.e., synchronously). This suggests that IBM's construction-which relies upon the phrase "from the point of view of the bus adapter, related data (i.e., a data word) is passed in a single operation over all of the SCSI buses at the same time" (the SCSI buses are the connections between the adapter and the disk drive units)-is correct. Moreover, because the SCSI protocol as contained in the patent lacks a command to synchronize multiple disks for reading and writing data in parallel, IBM's construction is not inconsistent with the prior art reference to the Boral article, which distinguished the '979 application as permitting asynchronous data transfer.

Thus, this second limitation will be described to the jury in the following terms:

Second, in the '979 patent, the data portions have to be "striped" in order to be stored. Now just what is "data striping?" Well, when you stripe data, you split it up so that sub-portions of the basic unit of data are stored in different storage units. To take a very simple example, if we think of the word "cat" as a data word, we would stripe that data word by taking it apart and placing one letter on each of three different disk drives. In order to figure out what the data word said, we would then have to read all three disk drives. By contrast, if you did not stripe the data, you would store all three letters of the word "cat" on the same disk drive.

So in this '979 patent, we have two or more data storage units, each one mechanically driven independently of the others, and each one of those data storage units stores one of those multi-bit portions of our data word. The multi-bit portions of the data word are thus said to be stored "in parallel." For this purpose, the data storage units have to have some way to write the data portions onto their storage media.

The patent claim specifies that each data storage unit stores "a respective one" multi-bit word portion. "A respective one" means exactly one, no more and no less. That means there must be an equal number of data storage units and multi-bit word portions in a system covered by the '979 patent. And the system needs to have the ability to transfer all of these multi-bit word portions over the connections between the disk drives and the adapter-the so-called SCSI buses-at the same time.

(iii) ... at least one correction bit storage unit including a storage medium that is mechanically driven independently from the mechanically-driven media on which said data word is stored, for storing an error correction code associated with said data words, said correction bit storage unit including as arrangement for writing correction bits onto its storage media ...

[19] The construction of this limitation necessarily follows from certain conclusions reached earlier. Because the claim clearly distinguishes between data storage units and error correction code units, I must advise the jury that the "correction bit storage unit" stores corrections bits, not any underlying data (even data that are not associated with a particular correction bit).

The other disputed element of this limitation concerns the meaning of the phrase "error correction code." IBM argues that this phrase has the same meaning as in the '342 patent, namely, it must both detect and correct data. TM says no, that this patent claim, unlike the '342 claim, says nothing about detecting as well as correcting data. This issue assumes particular importance in light of IBM's efforts to restrict the scope of this patent to so-called RAID 2 systems, which employ a Hamming code that both detects and corrects data errors.

As was the case with the '342 patent, I see no reason to restrict the scope of this patent to a system that employs Hamming code, even though the preferred embodiment shows the use of Hamming code. However, I am persuaded that the term "error correction code" in the '979 patent refers to a code that detects as well as corrects data, as it does in the '342 patent. The irrefutable support for this construction lies, not in the words of Claim 13, but in those of Claim 14, which is not alleged to have been infringed. Claim 14 of the '979 patent, which is dependent on Claim 13, refers to use of the "error correction code" in "a system as defined in Claim 13" to "perform[] an error detection and correction operation." FN6 And Claim 1 of the '979 patent also teaches that the error correction code is used to detect and correct.FN7 A term that appears in more than one claim must be interpreted the same way in each claim. *See Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1579 (Fed.Cir.1995); *Vitronics*, 90 F.3d at 1582; *Fonar Corp. v. Johnson & Johnson*, 821 F.2d 627, 632 (Fed.Cir.1987). Thus, the term "error correction code"-which means a code that both detects and corrects errors when used in Claims 1 and 14-must mean the same thing in Claim 13.

FN6. The relevant language of Claim 14 reads, " A system as defined in claim 13 in which the adapter generates correction bits for storage in said bit storage unit such that, if a data storage unit fails, *the adapter can, while performing an error detection and correction operation* with respect to each of said selected data words, determine a value for the data portion stored on the failed data storage unit" (emphasis added).

FN7. The relevant language of Claim 1 reads, "... an adapter connected to said parallel bus, said data storage units and said correction bit storage unit for, in response to a retrieval request, ... (iii) use the associated error correction codes to perform an error detection and correction operation."

This conclusion is buttressed by the prosecution history, during which claims that recited the function of "correcting errors" were rejected several times. (A 412-18, 431-35, 443-49.) In a response, applicants filed claims that explicitly called for detecting and correcting errors (A 456), and that is the language that appears in the claims themselves.

I will therefore instruct the jury as follows:

The third limitation is pretty self-evident from what we have said before. The system must include at least one storage unit-which means one storage unit or more than one storage units-that do not store any data, but rather are dedicated to storing error correction codes-which, as their name implies, are groups of bits that can correct an error. You will recall that we discussed error correction codes in connection with the '342 patent. In connection with that patent, I said that an error correction code both detected the presence of an error in the data and then corrected the error. And I gave you as an example of such a code, something called a Hamming code, which uses a group of bits to detect and correct error in the data associated with the code. In this patent, the term "error correction code" is used in the same way-that is, it is a code that both detects, which is to say, finds, any error in the underlying data associated with that particular code and then corrects that error in the underlying data. It is important to remember that every data word has its own corresponding error correction code.

(iv) ... an adapter connected to said parallel data bus, said data storage units and said correction bit storage unit for, in response to a storage request, (i) generating an error correction code for each data word, (ii) dividing each data word into a plurality of multi-bit portions, and (iii) transmitting said multi-bit portions and error correction code to respective data storage units and said correction bit storage unit for storage.

[20] [21] The last limitation appears easy to interpret on its face. Taken literally, it means that the system includes an adapter (elsewhere referred to as a controller), which is connected to three things: the parallel data bus (the multiple-wire conduit over which the data travels through the system), the data storage devices, and the correction bit storage unit. When the adapter receives a request to store new data, it causes three things to happen. First, it generates an error correction code for each data word that needs to be stored. Second, it divides the data word into two or more multi-bit portions (i.e., it "stripes" the data). Last, it sends the multi-bit portions and the associated error correction codes to their respective storage units.

IBM asks this Court to take a much less straightforward approach. It argues that this limitation ought to be construed in accordance with Section 112, para. 6 of the Patent Law, because it is a "means-plus-function" claim. I disagree with IBM and decline to impose means-plus-function status on this limitation.

We start from the proposition that a claim is presumptively not a means-plus-function claim when it does not use the talismanic words "means for ..." *See Personalized Media Communications Inc., L.L.C. v. Int'l Trade Comm'n*, 161 F.3d 696, 703-04 (Fed.Cir.1998). Of course, that is a rebuttable presumption, and IBM cites the Court to cases in which the Federal Circuit or a district court construed a claim that lacked the words "means plus." *See, e.g., Mas-Hamilton Group, Inc. v. LaGard, Inc.*, 156 F.3d 1206, 1214

(Fed.Cir.1998); *Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed.Cir.1983). IBM argues that limitation (iv) qualifies as a means-plus-function claim because it discloses nothing more than the function performed (an adapter that does x, y and z) rather than disclosing any structure. TM, supported by a greater number of cases, urges me to find that this limitation discloses enough structure, in addition to the functions performed, to keep the claim within the presumption.

To a neophyte like myself, this special wrinkle to the means-plus-function doctrine is particularly perplexing. TM correctly calls my attention to cases in which the following limitations have been held not to state means plus function claims: *Personalized Media*, 161 F.3d at 704-05 (finding that "digital detector" could not be construed as means-plus-function limitation; "detector" is not generic structural term, but rather had well-known meaning to those skilled in the art); *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed.Cir.1996) (Section 112 para. 6 could not apply to "detent mechanism" simply because claim took its name from function; "detent" had well understood meaning in the art); *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 531 (Fed.Cir.1996) (no means-plus-function treatment where claim described both structure and location); *Hay & Forage Indus. v. New Holland North America, Inc.*, 25 F.Supp.2d 1170, 1175 (D.Kan.1998) ("steering structure" did not state means-plus-function claim because structure was not just abstract means for performing a specified function, but specific device connected between junction box and tongue); *MediaCom Corp. v. Rates Technology, Inc.*, 4 F.Supp.2d 17, 27 (D.Mass.1998) ("switch jack" did not state means-plus-function claim where structure named and described as connected to adjacent structure). This last example is particularly difficult to understand, since the claim actually uses the "means plus" language.FN8 IBM responds that, in *MediaCom*, although the switch term was held not to be a means-plus-function, the construction of the term "switch jack" was nevertheless informed by the structure of the switch as described in the specification. *See MediaCom*, 4 F.Supp.2d at 27. IBM also notes that (1) in *Ethicon*, the Federal Circuit emphasized that it was not suggesting that paragraph 6 is triggered only if the word "means" is used; (2) the digital detector patent in *Personalized Media*, unlike the one in this case, included numerous embodiments; and (3) the *Hay & Forage* case has not been reviewed by the Federal Circuit.

FN8. Of course, just as the presumption of means-plus-function treatment for claims using means plus language is rebuttable, so also the converse: any presumption that the failure to use means plus language takes one out of the scope of Section 112, para. 6 can also be overcome.

IBM's clarifications notwithstanding, the examples cited by TM fairly support an argument that the claim in suit here is not a means-plus-function claim. The claim does not simply state "any means for performing functions x, y, and z." Rather, it discloses the use of an adapter (which TM asserts would connote a well-defined structure to persons of ordinary skill in the art), in a particular electronic configuration ("an adapter ... connected to said parallel data bus, said data storage units and said correction bit storage unit"), which performs those functions. If the cases cited by TM mean anything, it must be that the disclosure of this case is more than sufficient to keep a limitation out of the ambit of Section 112 para. 6.

IBM argues that the term "adapter" does not connote or identify any definite structure, but is rather a "generic descriptor" for "devices used to make electrical or mechanical connections between items not intended for use together." (IBM Br. at 23.) It calls the Court's attention to cases in which devices it deems similar have been found to state means-plus-function claims, notwithstanding the absence of the presumptive language. *See, e.g., Mas-Hamilton Group v. La Gard, Inc.*, 156 F.3d 1206, 1213-14 (Fed.Cir.1998) ("a substantially non-resilient lever moving element for moving the lever" qualifies as a

means plus function claim). And it suggests that the veracity of its position can be confirmed simply by replacing the word "adapter" with the word "means," so that the claim language reads "a means for" achieving the three desired functions.

However, IBM misreads the law. A claim qualifies for Section 112, para. 6 treatment when it covers *any* and all means for achieving a desired result. *See Davies v. United States*, 31 Fed.Cl. 769, 776 (Fed.Cl.1994). Thus, the "lever moving element for moving a lever" in *Mas-Hamilton* encompasses anything that can be used to make a lever move. It is a tautological claim. The instant claim is not. It does not cover any conceivable means for dividing the data words, generating error codes and sending the data and associated error codes on their respective ways. It covers one means: an adaptor that is simultaneously connected to both types of storage units (data and error correction bit) and to the parallel bus. If this could be converted into a means-plus-function claim, then so could any claim in which the disclosed structure takes its name from the function it performs, e.g., "brake", "clamp", or "filter," to name a few.

I therefore decline to construe this claim under Section 112, para. 6, and I reject IBM's suggestion that it be defined for the jury in terms of the specifications disclosed in the preferred embodiment. I will explain the claim to the jury in the precise terms set forth in the opening paragraph of this section of the opinion.

C. The '773 Patent

The '773 patent concerns a different technology than the '342 and the '979 patents. We have moved into the area of something called massively parallel processing, which is the use of several processors to work on discrete parts of a data problem at the same time. The '773 patent is for a message routing network that transmits messages from point A to point B in a particular fashion via a message routing network. A message routing network is organized as a collection of nodes (which I think of as way stations) and communications links (wires or conduits along which information travels from point A to point B). The communications links carry the message from one place to another, and the nodes connect the communications links together.

The '773 patent teaches a particular computer message routing system that uses a technique that the parties refer to as "wormhole routing." Plaintiffs contend that "wormhole routing" can best be understood by contrasting it with other message routing techniques, and I agree. Wormhole routing appears to be a significant improvement over other forms of message routing, such as circuit-switching (an extremely slow process in which every component of a path from point A to point B—that is, all the wires to be traversed and all the nodes to be gone through—must be established (set) before any part of the message can leave point A on its way to point B); "store-and-forward" (in which the entire message, from the head, which contains the address, to the tail, or the end, must arrive at a particular node before any part of the message can begin moving on to the next node—even if the next node in line is free and ready to begin accepting transmission); or "cut-through" (in which the head of a message will "flow through" to the next node in sequence without waiting for its tail to catch up to it, unless the next node is busy, in which case the head must sit in a message buffer until the entire message catches up to it before it can be sent on to some other node). In wormhole routing, however, when the head of a message arrives at one node it is sent on to the next appropriate node as soon as that output location is identified. If the appropriate output circuit is not available, the head of the message will be stored in a buffer, but it will leave the buffer and start moving again as soon as an output circuit becomes available—whether or not the tail has caught up to it. Thus, the message may extend over a number of nodes at any given time.

TM obviously believes that it has patented wormhole routing and argues for a claim construction that is extremely expansive. IBM contends that TM has patented a means-plus-function system and seeks to have me limit the patent to the very components used in the preferred embodiment. Not surprisingly, I come down somewhere in the middle.

1. Construction of Disputed Claims

(a) Claim No. 1-Disputed Elements

The key issue is whether this independent claim must be construed in light of Section 112, para. 6. Just about every decision I must make hinges on that determination. I conclude that Claim Number 1 is not a means-plus-function claim. However, I prefer to follow the same format as with the two other patents, and will therefore address myself to the disputed limitations seriatim.

(i) A computer system comprising a plurality of processing elements and a message router in which: (A) each processing element for generating messages, each message comprising an address portion comprising a series of address elements and a data portion comprising at least one data element, each processing element including a message transfer circuit for transmitting messages over said message router and for receiving messages from said router, said message transfer circuit transmitting each message by serially transmitting address elements and a data element thereof and receiving a message by serially receiving at least a data element thereof;

The first and most important thing to note about this limitation is that it refers to a computer system consisting of certain hardware (two or more processors and a message router), not to a process (wormhole routing). To that extent, IBM is correct: TM has not patented wormhole routing, but rather a system for accomplishing that result. Of course, equivalents of that system will also infringe the patent, but that is a question best left for another day.

Each processing unit in the system-which everyone agrees is any processor that can generate messages-is used to generate messages. Each message consists of an address portion and a data portion. There can be as little as one bit of data in the data portion, but the address portion must consist of multiple bits. The limitation does not require that the address consist of just one element; any such construction is contradicted by both the plain meaning of the language used in the limitation (a "series of address elements") and the fact that a later dependent claim (Claim 6) requires that "each address element in each said message constitutes one bit."

The processor must contain a message transfer circuit which can both send and receive messages to and from the message router. The transfer circuit sends messages by serially transmitting the address elements and any data element (serially meaning in sequence, one element after another). It receives messages by serially receiving at least the data portion of the message (this is because the address gradually gets stripped off the head of the message as it moves through the system, so the last processor in line will not receive any portion of the address).

IBM suggests that the use of the phrase "message transfer circuit" in this limitation (and later ones as well) transforms it into a means-plus-function limitation, and is therefore restricted to the specific communications interface unit shown at Figures 6B and 8 of the patent. TM has the better of this argument. Claim 1.A is not a claim for a message transfer circuit, but for a computer system having as one of its component parts a message transfer circuit that does certain things. In other words, the phrase "message

transfer circuit" refers to a structure within the computer system. That this structure has a particular function to perform, and must therefore be capable of performing that function, does not transmute a structural component of a computer system into a means-plus-function claim to which Section 112, para. 6 applies.

TM has not here attempted to patent an unspecified "means for routing messages through a computer system without forcing the head of the message to wait for the tail." It cannot be expected to recite an invention without identifying its component parts. Interestingly, TM tried to do so; the prosecution history shows that claim 2 of the preliminary amendment to this patent (which was ultimately canceled) recited "means for serially transmitting message elements and means for serially receiving message elements." (A 2089.) That is not how the patent ended up. As allowed by the Examiner, it requires the use of a circuit to transfer messages. Other courts have held the word "circuit" to be a structural term, *see, e.g.,* CellNet Data Systems, Inc. v. Itron, Inc., 17 F.Supp.2d 1100, 1107 (N.D.Cal.1998). Its dictionary definition-which IBM cites-is "An electrical network in which there is at least one path that can be closed," S. Handel, *A Dictionary of Electronics* 59 (2d ed.1966), or, alternatively, "A complete wire, radio or carrier communications channel." *McGraw Hill Dictionary of Scientific and Technical Terms* 302 (3d ed.1984). Neither of those is a functional definition. Yes, it is a circuit that transfers messages-that is its function in the invention-but the fact that a disclosed structural element has a function should surprise no one. Under IBM's reasoning, nearly every patent limitation would qualify for Section 112 para. 6 treatment.

(iii) a switch connected to said input circuits for, for each message received by said input circuits, decoding one address element of the message to identify therefor an output circuit, said switch establishing a path for said message between the input circuit which received the message and the identified output circuit to facilitate the transfer of message elements of said message therebetween, said switch maintaining the path until the last of the serially-received message elements for the message have been transferred to the identified output circuit.

[22] These three limitations, considered together because of their interrelatedness, are the heart of the computer system contemplated in the invention, and the parties spent most of their time at the *Markman* hearing disputing the meaning of the terms "switch," "establishing the path," and "maintaining the path."

IBM's primary argument with regard to these limitations is identical to its argument concerning the message transfer circuit-it contends that TM's use of the word "switch," which it believes to be amorphous as to structure, converts this part of the claim into a means-plus-functionclaim that is subject to the strictures of Section 112, para. 6. Again, I disagree, and for the same reasons as outlined above. A switch is commonly understood to be a structure. It is a device for making, breaking, or changing connections in an electrical circuit. Like the word "brake," "clamp," or "screw," the name of the device connotes what it does. The commonly understood meaning of the word is cast in terms of its function. It is well settled that naming a function-specifying device in a patent claim is not sufficient to bring that claim within the ambit of Section 112, para. 6. *See* Ethicon Endo-Surgery, 91 F.3d at 1583; Implant Innovations, Inc. v. Nobelpharma AB, No. 93 C 7489, 1998 WL 704188, (N.D.Ill. Oct. 1, 1998).

TM did not patent a better means for making, breaking, or changing connections in an electrical circuit. It patented a computer system that is configured so as to route messages more efficiently. One of that system's component parts is a switch-a switch that must be able to decode, establish, and maintain a path through the system. The switch is the structure that is used to accomplish a certain result. It is incorporated into the system in a particular way-by connecting it to the input circuits, which are in turn connected to the communications links. This is more than sufficient for me to reject IBM's argument-and with it, IBM's

contention that the scope of this limitation is no broader than the embodiment disclosed in the patent.

I agree with TM that, in the Examiner's statement about "the router node as currently claimed and in the structure as currently claimed," the word "structure" refers to the computer system. I do not agree with IBM that this phrase indicates any intention on the part of the examiner to construe the limitation as a means-plus-function limitation. I also reject IBM's argument that I should construe "switch" in means-plus-function terms because the specifications do not use the word "switch." IBM cites no authority for that proposition, and as a matter of logic it makes no sense.

The path to be established by the switch must run from the input circuit that received the message to the "identified" output circuit. The switch "identifies" that output circuit by decoding some portion of the address element at the head of the message in order to determine the message's destination. The parties agree that "decoding" means examining and translating, or analyzing.

[23] IBM argues that the switch as disclosed in the claim should be limited to one that decode exactly one, and no more than one, address element. TM contends that this is one of those instances when "one" means "at least one" or "one or more than one," and points out that the preferred embodiment would be excluded if the limitation IBM urges were read into the claim. As TM notes, claim interpretation that would exclude the preferred embodiment is "rarely, if ever, correct and would require highly persuasive evidentiary support." *Vitronics*, 90 F.3d at 1583. TM also argues that a switch that decodes more than one element of an address would necessarily infringe the patent, because it would have to decode "one" in order to decode "more than one."

IBM's evidence for a contrary result is not unpersuasive. First, the literal meaning of "one" is singular, not singular and/or plural. Despite the fact that "a" and "an" can apparently mean either the singular or the plural, at least in the patent context, *see North Am. Vaccine v. American Cyanamid Co.*, 7 F.3d 1571, 1575-76 (Fed.Cir.1993) (citing Robert C. Faber, *Landis on Mechanics of Patent Claim Drafting* 531 (3d ed.1990)); *Shell Oil Co. v. ICI Americas, Inc.*, 33 F.Supp.2d 523, 525-26 (E.D.La.1999); *Isogon Corp. v. Amdahl Corp.*, No. 97 Civ. 6219 SAS, 1998 WL 901723, (S.D.N.Y. Dec. 28, 1998), there are plenty of ways to phrase something if both the singular and the plural are intended to be encompassed ("one or more," "one or more than one," and "at least one" all come to mind). Especially in light of the Federal Circuit's recent pronouncement on the subject, *see WMS Gaming, Inc. v. Int'l Game Tech.*, Nos. 97-1307, 98-1053, 1999 WL 508800, (Fed.Cir. Jul. 20, 1999), the meaning of the word "one" would seem to be a very straightforward proposition.

Assigning a singular meaning of "one" seems all the more reasonable in light of the fact that claims canceled during prosecution of the '773 patent contained the phrase "at least one," while the eventual language of the patent is limited to "one." TM correctly notes that this matters to claim construction only if the particular language focused on is altered in order to escape an examiner's rejection. *See York Products, Inc. v. Central Tractor Farm & Family Center*, 99 F.3d 1568, 1574 (Fed.Cir.1996). However, TM's argument for why this particular alteration was of no consequence to overcoming the rejection—namely, that the patentee "would have known that 'at least one' and 'one' were synonymous" (TM Reply Br. at 36)—is neither self-evident nor particularly persuasive. Indeed, placing this limitation as originally filed side-by-side with the limitation as eventually allowed, it seems that the only substantive alteration was changing "at least one" to "one." Of course, this particular phrase is only part of the claim, and IBM conceded at argument that there are other differences between the patent as filed and as allowed. (*See Tr. of Markman Hearing*, Sep. 8-9, 1999, at 346.)

Finally, IBM argues that the claims calling for the decoding of "at least one" address element were rejected over the prior Lawrence '892 patent, and urges that this very phrase was the reason. It cites the Court to the appendix (A 2163-87) in support of its argument. In response, TM, citing the Examiner's Statement of Reasons for Allowance (A 2113), contends that this change was not the reason for the rejection. It points out that the Examiner said that the router node "will establish and maintain, *after it receives enough of a message* [which TM interprets to mean *not just one element of a message*] *to determine an output circuit over which it will transmit the message*, a path from the input circuit to the output circuit until the entire message has been established" (emphasis added).

I have reviewed the cited portions of the Joint Appendix, especially Figure 15 and its corresponding description at A 2183, and I find that they shed very little light on the subject. It seems to me, however, that the single most persuasive piece of evidence on this point is the statement of the Patent Examiner himself. If his reason for rejecting the claim as initially filed was TM's use of the phrase "more than one" rather than "one," it is difficult to understand why he would have stated that the router node transmits the message "after it receives *enough of a message* to determine the output circuit ..." (emphasis added). The words "enough of a message" are not limited to a single address element, and it would have been easy enough for the Examiner to say what he meant if he intended to so limit the invention. His choice of words seems especially pertinent because both parties agree that the preferred embodiment calls for the switch to decode more than one element. IBM is correct that there are occasions when it is both necessary and appropriate to construe a patent claim in a way that reads the disclosed embodiment out of the patent. *See Ultra-Temp v. Advanced Vacuum*, 11 F.Supp.2d 141, 147 (D.Mass.1998). This, however, does not seem to me to be such a case.

While the question is a close one, and IBM's presentation is impressive, especially as to the file wrapper estoppel point, I do not find the evidence supporting its argument to be "highly persuasive," as required by *Vitronics*. *See Vitronics*, 90 F.3d at 1583. I am therefore inclined to interpret "one" as encompassing both the singular and the plural. I confess that I reach this particular conclusion without much confidence (a la Judge Young in the *EMC* case), and I invite the parties to submit for my consideration anything that they have *not already called to my attention* that they believe would either buttress my holding or undermine it. It would be infinitely more helpful if the parties could cite me to a single item of correspondence from the Examiner to the patentee articulating the reasons why he disallowed the initial claims. To date, they have not done so.

That the path must run from the input circuit to the very output circuit that was identified in the decoding process is evident from the plain language of the limitation. It admits of no other interpretation. If that identified circuit is busy, then the head of the message must proceed to a message buffer, which will be discussed later. It cannot be sent to some alternate address.

[24] I now turn to the next disputed elements of this limitation, which are "establishing" and "maintaining" the path for the message to travel. There is really no dispute about the term "establishing." When the switch establishes a path for the message to travel, it "decides" where the message has to go. IBM puts it quite plainly: the switch sets up a path for the message to travel from the input circuit that received the message to the output circuit that was identified during the decoding process. When it does that, the switch "establishes" the path. It is fixed and will not be changed.

The word "maintains" generates considerably more controversy. As IBM notes, the parties are in agreement

to a certain extent. They agree that, once the output circuit has been identified and the path established, that path may not change during the time the message is transiting (going through) the switch. By the end of oral argument, it became clear that the parties also agreed that the notion of a second message's cutting across (or interleaving) that path was inconsistent with the concept of "maintaining" the path. No other message can cut in, or ditch, the message whose path has been established once that path is established.

The parties do not agree, however, about whether two or more messages can occupy the same path at the same time. TM contends that its claim is broad enough to encompass such a situation, although I infer that a technology that would permit two messages to travel the same path at the same time has not yet been invented. IBM contends that simultaneous transmission of messages is not disclosed in the patent and that lack of exclusivity is inconsistent with the concept of "maintaining" a path for the use of our message until the entire message has passed over the wire.

The dictionary definition of the word "maintain" is "to preserve or keep in a given existing condition." *Webster's II New Riverside University Dictionary* 717 (1994). As no one disputes that the path in question must be kept in a state of readiness to transmit the message from the time it is established until the entire message has passed through, I find that this definition is not particularly helpful concerning the precise issue confronting me. Neither are any of the other dictionary definitions proffered by IBM in its Glossary of Terms.

I turn then to the specifications, which, as IBM observed repeatedly during the *Markman* hearing, are the single best guide to interpreting claim language. (Tr. of *Markman* Hearing at 96-97, 112, 300). The specification clearly and unmistakably states that the path established is for the *exclusive* use of the message. (*See* '773 Patent, column 2, lines 49-56, attached as Exh. C to Cmplt.) Such an interpretation is logically consistent with the notion of the path's being "maintained" for the particular message we are analyzing. It is also consistent with the notion, contained in Claim 2, that messages must be buffered (put in a waiting area, so to speak) if a path to their destination output circuit is occupied. If two or more messages could occupy the same path at the same time, there would be no need for a buffer in which to store one message while another occupies the path.

I am not persuaded by TM's argument that Claim 1 does not require exclusivity because the dependent claim, Claim 2, does not require exclusivity. Claim 2, to my reading, clearly does require exclusivity. Similarly, after reading the parties' supplemental submissions, I am not persuaded that the doctrine of claim differentiation applies here, since both Claim 1 and Claim 2 recite the words "establish" and "maintain." As IBM points out, claim differentiation presumes a difference in meaning and scope when different words or phrases are used in separate claims; it does not permit the same words to be construed differently in different limitations. *See Tandon v. International Trade Commission*, 831 F.2d 1017, 1023 (Fed.Cir.1987); *Slater Electric, Inc. v. Thyssen-Bornemisza Inc.*, 650 F.Supp. 444, 463-64 (S.D.N.Y.1986).

I therefore accept IBM's argument and construe the word "maintaining" to require the path to be kept free for the exclusive use of a particular message.

I defer putting this construction in the precise language I will use with the jury until such time as I have come to a final decision on the one issue that still troubles me, which is the proper meaning of the word "one." The parties will have ample opportunity to critique my opening charge before it is delivered (though they should keep their comments to the clarity of the language and its consistency with this opinion, and not use that opportunity to reargue positions I reject here).

(b) Claim No. 2 (Dependent Claim)-Disputed Limitations

[25] Claim 2, which is a dependent claim, recites the computer system as defined in Claim 1 and then adds a new element: a "message buffer," which is connected to the switch. The buffer works as follows: if the switch has already established a path for a message to run from Input Circuit A to Output Circuit B, and Input Circuit C receives a message that is also addressed to Output Circuit B, then the switch will establish a path from Input Circuit C to the message buffer. The second message in line will proceed to the buffer, which the parties agree is a place where messages wait until their path is clear. It is my understanding that the head of the message will proceed out of the buffer toward the designated output circuit as soon as that circuit is free to receive it; the head need not wait until the entire message has been received at the buffer.

This language presents no interpretive problems. IBM argues that the "message buffer" must have sufficient capacity to store an entire message, claiming that it would be a misnomer to call anything smaller a "message buffer." This is hardly a persuasive argument. While it might be desirable to have an amply-sized buffer, there is absolutely nothing in the claim language that requires it.

I anticipate that I will use the language in the first paragraph of this section (b) in my charge to the jury.

This constitutes the decision and order of the Court.

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