United States District Court, N.D. California.

XILINX, INC, Plaintiff. v. ALTERA CORPORATION, Defendant. ALTERA CORPORATION, Plaintiff. v. XILINX, INC, Defendant.

No. 93-20409 SW, 96-20922 SW

July 30, 1998.

### **CLAIM CONSTRUCTION ORDER**

#### WILLIAMS, J.

### I. BACKGROUND

On June 7, 1993, Xilinx, Inc. ("Xilinx") initiated Civil Action No. 93-20409 against Altera Corporation ("Altera") alleging infringement of U.S. Reissue Patent No. 34,363 ("the '363 patent") and U.S. Patent No. 4,642,487 ("the '487 patent"). On August 8, 1996, this action was reassigned to this Court.

On June 7, 1993, Altera initiated a separate action against Xilinx alleging infringement of U.S. Reexamination Patent No. B1 4,617,479 ("the B1'479 patent"), and U.S. Patent Nos. 4,774,421 ("the '421 patent") and 4,609,986 ("the '986 patent"). FN1 The specification of the '986 patent incorporates by reference the specification of the B1'479 patent. Altera's action against Xilinx was ultimately given case number Civil No. 96-20922, and on November 7, 1996, was reassigned to this Court.

FN1. Altera also initially alleged infringement of U.S. Patent No. 4,020,469 but has since withdrawn that allegation.

This Court deemed the two actions related and on December 11, 1996, ordered that a joint claim construction hearing be held for both actions. On October 20-23, 1997, the Court conducted the claim construction hearing for the five patents at issue. During the hearing, the parties presented tutorials, offered evidence and made arguments for the purpose of aiding the Court in construing the disputed terms used in the claims. Following the hearing, the parties submitted additional briefs in support of their proposed

constructions.

## **II. LEGAL STANDARD FOR CLAIM CONSTRUCTION**

Determining patent infringement requires a two-step analysis: "First, the claim must be properly construed to determine its scope and meaning. Second, the claim as properly construed must be compared to the accused device or process." Nike Inc. v. Wolverine World Wide, Inc., 43 F.3d 644, 646 (Fed.Cir.1994) (quoting Carroll Touch, Inc. v. Electro Mechanical Systems, 15 F.3d 1573, 1576 (Fed.Cir.1993)). Claim construction is a matter of law to be determined by a court. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed.Cir.1995), *aff'd*, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). The comparison between the properly construed claims and the device accused of infringing is a question of fact. General Mills, Inc. v. Hunt-Wesson, Inc., 103 F.3d 978, 981 (Fed.Cir.1997).

# A. Evidence

In construing the meaning of claims, courts first consider a patent's intrinsic evidence, which includes the claims, the specification, and the prosecution history. Markman, 52 F.3d at 979. The patent title may be considered as an interpretive aid. *See* Exxon Chemical Patents, Inc. v. Lubrizol Corp., 64 F.3d 1553, 1557 (Fed.Cir.1995). In addition to intrinsic evidence, the parties may offer extrinsic evidence which includes expert testimony, inventor testimony, dictionaries and learned treatises. Markman, 52 F.3d at 980. Although a court may consider extrinsic evidence, it should look first to the intrinsic evidence of record. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996).

When considering the intrinsic evidence courts are to look first to the claims themselves to define the scope of the invention. Id. at 1582. Generally, the words in a claim are given their ordinary and customary meaning. *Id.* However, "a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the specific definition of the term is clearly stated in the patent specification or file history." *Id.* Thus, the specification may act as a dictionary when it expressly or impliedly defines terms used in the claims. *Id.* Furthermore, the file history is often critical in determining the meaning of the claims. Any interpretation that was disclaimed during the prosecution must be excluded from the definition of claim terms. Southwall Tech., Inc. v. Cardinal IG Co. ., 54 F.3d 1570, 1576 (Fed.Cir.1995), *cert. denied*, 516 U.S. 987, 116 S.Ct. 515, 133 L.Ed.2d 424 (1995).

"In most situations, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term. In such circumstances, it is improper to rely on extrinsic evidence." Id. at 1583. Only when intrinsic evidence alone is insufficient may the court use extrinsic evidence, and then only to aid the court in "coming to the proper understanding of the claims" and the technology involved. Id. at 1584. Extrinsic evidence may not be used to vary or contradict the claim language. Markman, 52 F.3d at 981. Expert testimony is to be eschewed and used only as a last resort. Vitronics, 90 F.3d at 1584-85. The Federal Circuit in *Vitronics* showed a clear preference for other types of extrinsic evidence, such as dictionaries and prior art documents. *Id.* at 1585.

## **B.** Means-plus-function Claim Elements

As a general principle of claim construction, limitations found in the specification of a patent should not be read into a claim. In re Donaldson Co., 16 F.3d 1189, 1195 (Fed.Cir.1994). However, claim elements expressed as a means or step for performing a specified function are construed to cover the corresponding "structure, material or acts described in the patent specification" and their "equivalents." 35 U.S.C. s. 112,

para. 6. Under a means-plus-function analysis, if the specification mentions specific alternative structures, those structures are included in the scope of the patent. *See* Serrano v. Telular Corp., 111 F.3d 1578, 1583 (Fed.Cir.1997). A specification that merely mentions the possibility of alternative structures without specifically identifying them is not sufficient to expand the scope of the claim beyond the example used. *See* Fonar Corp. v. General Electric Co., 107 F.3d 1543, 1551 (Fed.Cir.), *cert. denied*, 522 U.S. 908, 118 S.Ct. 266, 139 L.Ed.2d 192 (1997).

"In determining whether to apply the statutory procedure of section 112, para. 6, the use of the word 'means' triggers a presumption that the inventor used this term advisedly to invoke the statutory mandates for means-plus-function clauses." York Prods., Inc. v. Central Tractor, 99 F.3d 1568, 1574 (Fed.Cir.1996). However, "[t]o invoke this statute, the alleged means-plus-function claim element must not recite a definite structure which performs the described function." Cole v. Kimberly-Clark Corp., 102 F.3d 524, 41 U.S.P . Q.2d 1001, 1006 (Fed.Cir.1996). "An element with ... a detailed recitation of structure, as opposed to its function, cannot meet the requirements of the statute." *Id*. Whether the procedure of s. 112 para. 6 applies should be decided "on an element-by-element basis, based upon the patent and its prosecution history." *Id*.

## C. "Jepson" Claims

A "Jepson" claim is one that contains (1) a preamble that recites an old device, process, or combination, (2) a transition phrase such as "wherein the improvement comprises," and (3) a body which states the new elements or improvements upon the old device, process, or combination. *See* 37 C.F.R. s. 1.75(e); *see also Ex parte Jepson*, 1917 C.D. 62 (Ass't Comm'r Pat.1917). The preamble in a Jepson claim constitutes "a limitation for purposes of determining patentability and infringement." 3 Donald S. Chisum, *Chisum on Patents* s. 8.06[1][c], at 8-104 (1998); *see also Manual of Patent Examining Procedure*, s. 608.01(m) (6th ed.2d rev.1996) ("The preamble of [a Jepson claim] is considered to positively and clearly include all the elements or steps recited therein as a part of the claimed invention."; Pentec, Inc. v. Graphic Controls Corp., 776 F.2d 309, 315 (Fed.Cir.1985) ("Although a preamble is impliedly admitted to be prior art when a Jepson claim is used, ... the claimed invention consists of the preamble in combination with the improvement.") (citations omitted).

## **III. DISCUSSION**

The Court has very carefully examined the claims and the proposed constructions offered at the claims construction hearing. In addition, the Court has employed the assistance of the independent technical advisor in fully understanding the technology pertinent to the patents in suit. *See* Order re: Duties of the Technical Advisor, dated July 17, 1997. The Court reiterates that the technical advisor has not contributed evidence or rendered conclusions of law. Furthermore, the technical advisor has offered no opinion regarding any legal issues in this action, including opinions on the validity of the patents in suit or whether any of the contested patent claims are infringed by the accused products.

Although the Court permitted extrinsic evidence at the claim construction hearing, the Court construes the claims without consideration of extrinsic evidence except as explicitly noted below. Furthermore, the Court notes that although Xilinx urged the Court to construe portions of the claims of the original '479 patent, the Court construes only the disputed claims of the reexamined B1'479 patent, taking into consideration the claim language and file history of the original patent. What follows is the claim language and the Court's construction thereof for each disputed claim.

The '363 Patent

Patent '363 Claim 11	Construction
A configurable system	A configurable system
	is one
comprising:	or more devices
	connected
	together that can be
	configured to perform
	different functions.
One master	A configurable logic
configurable logic	array
array;	("CLA") is a circuit
	containing configurable logic
	elements which can be
	connected to each other and to
	inputs and outputs if
	anv.
	through a configurable
	interconnect structure
	See
	in passim 1:64-2:46. <sup>2</sup>
	A configurable logic
	element
	("CLE") is "a
	combination of
	devices which are
	capable of
	being electrically
	interconnected by switches
	operated in response to
	control bits to perform any
	one of a plurality of logical
	functions." 1:59-63.
	A master CLA is one which
	"initiates the transfer of

the

	information for
	controlling or
	configuring the CLA
	from the
	non-volatile memory to
	the
	master CLA and to the
	slave
	CLAs" as described
	below.
	11:50-53. See Fig. 8B.
a plurality of slave	A slave CLA is one
	which
configurable logic	receives configuration
arrays;	data
	from the master. The
	system
	must have more than
	one slave
	CLA.
at least one memory;	A memory is a device
	external
	to the configurable
	logic
	arrays which is capable
	of
	the
	configuration data
	necessary
	to configure the CLAs
	of the
	system.
said master	The master CLA must
configurable logic	have a
array having means for	structure which is the
	same as
retrieving data from said at	or the equivalent of the
least one memory,	structure in the
	specification
	which performs the
	function of
	retrieving data from the

	memory. The structure
	disclosed in the
	specification
	is: standard circuitry
	that
	generates address
	signals and
	a control signal; ports
	to
	communicate those
	signals
	outside of the array;
	and a
	port to receive
	configuration
	data from a source
	external to
	the array. See Fig. 8B.
means for first using	The master CLA must
said	have a
data for configuring	structure which is the
itself,	same as
and	or the equivalent of the
	structure in the
	specification
	which performs the
	function of
	using the retrieved data
	for
	configuring itself first.
	А
	CLA is configured
	when the
	combination of
	configured CLEs
	and the interconnect
	structure
	yields a desired logical
	output. 6:17-20. A CLE
	is
	configured when it is
	capable
	of performing a desired
	logic

	function. 6:41-42. The
	structure disclosed in
	the
	specification which
	uses the
	retrieved data for
	configuring
	itself first is the RAM
	of
	Figure 3A, the RAM of
	Figure
	3B, or the dynamic shift
	register-static latch of
	Figure 5 operating in
	its
	static latch mode. 5:64-6:2;
	7:66-8:4; see Figs. 3A,
	3B,
	and 5.
means for passing	The master CLA has a
some of said	structure
data to said plurality	which is the same as or
of	the
slave configurable logic	equivalent of the structure in
arrays.	the specification which
-	performs the function of
	passing some of the retrieved
	data to the slave CLAs. The
	structure disclosed in
	the
	specification is:
	standard
	circuitry that generates
	а
	data clock signal; a port
	$\omega$
	signals from
	the master to the

ule master to the slaves; and	
a port to communicate data	
signals from the master	ſ
to the	
first slave. Fig. 8B.	

FN2. Citations to the patent specification are of the form column: line. For example, 1:64-2:46 refers to column 1 line 64 through column 2 line 46. Unless otherwise noted, all citations to the specification refer to the patent from which the disputed language originates.

Patent '363 Claim 21	Construction
A programmable	A programmable circuit
circuit	is a
comprising:	circuit which is capable
	of
	being programmed to
	perform
	different functions.
a plurality of	See discussion of CLE
configurable	in claim
logic elements,	11 above. The circuit
	must
	have more than one
	CLE.
each configurable	An input lead is a
logic	structure
element having a	that can be used to input
plurality of	a
input leads and at	signal to a CLE. Each
least one	CLE
output lead and	must have more than
having	one input
	lead. An output lead is a
	structure that can be
	used to
	output a signal from a CLE.
	Each CLE must have at
	least
	one output lead. See e.g.
	Figs. 2, 3A, 3B, 4A & 7A.
a programming means	A structure which is the
to cause	same
said configurable	as or the equivalent of

logic element to perform a selected logic function;

the structure in the specification which performs the function of causing a CLE to perform a selected logic function. The structure disclosed in the specification is the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch operating in its static latch mode. 5:64-6:2 ("To program the circuitry of a logic element such as shown in Figure 2 selected signals are applied to input leads of the configurable logic element identified as configuration control input leads from а source such as the RAM of FIG. 3A or 3B described above thereby to generate a desired logical function in each of the logic elements"); 7:66-8:4; see Figs. 3A, 3B, and 5.

a plurality of input/output	An input/output port is a
ports;	structure that can be used to
	input a signal, output a
	signal, or both, to or
	from
	the programmable
	circuit.
	12:65-68 and Fig. 4A.
a group of interconnect lines;	Interconnect lines are
	structures, regardless of
	their length, which conduct
	data signals from place
	place within the
	integrated
	circuit device. See, e.g.
	Fig. 7A (LL1, LL2, L1, L2).
means for	A structure which is the
programmably	same
connecting each of said input	as or the equivalent of the
leads of each of said	structure in the specification
configurable logic	which performs the
elements to	function of
at least one of said	programmably connecting CLE
interconnect lines;	input leads to
	lines. The structure
	disclosed in the
	is the DAM of Figure
	3A, the
	RAM of Figure 3B, or
	the
	dynamic shift register- static
	latch of Figure 5

	operating in
	its static latch mode,
	and the
	pass transistors it
	controls.
	5:64-6:2; 6:38-48; 7:40-
	43;
	7:66-8:4; see Figs. 3A,
	3B, 5,
	7B, and 9A-G.
means for	A structure which is the
programmably	same
connecting said at	as or the equivalent of
least one	the
output lead of each of	structure in the
said	specification
configurable logic	which performs the
elements to	function of
at least one of said	programmably
	connecting CLE
interconnect lines;	output leads to
	interconnect
	lines. The structure
	disclosed in the
	specification
	is the RAM of Figure
	3A, the
	RAM of Figure 3B, or
	the
	dynamic shift register-
	static
	latch of Figure 5
	operating in
	its static latch mode,
	and the
	pass transistors it
	controls.
	5:64-6:2; 6:38-48; 7:40-
	43;
	7:66-8:4: see Figs. 3A.
	3B, 5,
	7B, and 9A-G.
means for	A structure which is the
programmably	same

connecting each of	as or the equivalent of
said	the
input/output ports to	structure in the
at least	specification
one of said	which performs the
interconnect	function of
lines; and	programmably
	connecting
	input/output ports to
	interconnect lines. The
	structure disclosed in the
	specification is the
	$\begin{array}{c} \text{KANIOI} \\ \text{Figure 3A}  \text{the PAM of} \end{array}$
	Figure SA, the KAW of
	3B, or the dynamic shift
	register-static latch of
	Figure 5 operating in its
	static latch mode, and
	the
	pass transistors it
	controls.
	5:64-6:2; 6:38-48; 7:40-
	45; 7.66 8.4. and Eige 2.4
	7:00-8:4; see Figs. 5A, 3B 5
	7B, and $9A$ -G.
means for	A structure which is the
programmably	same
connecting each one	as or the equivalent of
of said	the
interconnect lines to	structure in the
at least	specification
one other of said	which performs the
lines	neogrammably
mies,	connecting
	interconnect lines to one
	another. The structure
	disclosed in the
	specification
	is the RAM of Figure
	3A, the
	DAM of Eigung 2D on

	KAINI OF FIGURE 3D, OF
	dynamic shift register-
	static
	latch of Figure 5
	operating in
	its static latch mode,
	and the
	pass transistors it
	controls.
	5:64-6:2; 6:38-48; 7:40-
	43;
	7:66-8:4; see Figs. 3A,
	3B, 5,
	7B, and 9A-G.
whereby each of said	Connected directly
input	means that
leads and each of said	a connection can be
at	made
least one output lead	solely via interconnect
of each	lines,
logio	a CLE
alemente con he	a CLE.
connected	means
directly or indirectly	that a connection must
to each	pass
of said input/output	through a CLE. Patent
ports and	File
to each other, and	History, Amendment in
whereby	Response
each of said	to 2nd Office Action,
configurable	Jan. 13,
logic elements can be	1993 at 17-18; Patent File
programmed to	History, Notice of
perform a	-
selected one of a	Allowability, Feb. 2,
plurality of	1993 at
logic functions, and	2.
said	
configurable logic	
elements	
can be connected to	
each other	

and to said

anu io saiu	
input/output ports	
in a selectable manner.	
Patent '363 Claim 22	Construction
A programmable circuit	See claim 21.
as in	
claim 21	
wherein said	See discussion of
programming means	"programming
of each of said	means" in claim 21
configurable	above. The
logic elements	"programming means"
comprises logic	element of
element pass transistors.	each CLE must include
Ĩ	logic
	element pass transistors.
Patent '363 Claim 23	Construction
A programmable circuit	See claim 22.
as in	
claim 22	
wherein said	See discussion of
programming means	"programming
includes a plurality of	means" in claims 21
memory	and 22
cells	above. The
	"programming
	means" element of each CLE
	must include more than
	one
	cell of the RAM of
	Figure 3A,
	the RAM of Figure 3B,
	or the
	dynamic shift register-
	static
	latch of Figure 5
	operating in
	its static latch mode.
and wherein each of said logic	Each logic element pass
element pass transistors	transistor must be
is	controlled
controlled by a	by one of the cells
corresponding	described

one of said plurality of	above.
memory cells.	
Patent '363 Claim 24	Construction
A programmable	See claim 23.
circuit as in	
claim 23	
in which said	The memory cells
plurality of	must be
memory cells forms	arranged so as to
at least	form at
part of a shift	least part of a shift
register,	
	register. See Fig. 5.
control signals being	Control signals are
loaded	to be
into said memory	loaded into the shift
cells by	register
being transferred	by transferring
through said	(shifting)
shift register until	those signals from
each of	one cell to
said signals is	the next within the
properly	shift
located in said	register until the
corresponding	signals are
one of said memory	in their proper
cells.	locations.
Patent 303 Claim 25	Construction
A programmable	See claim 23.
clicuit as in	
in which sold more any	The memory cells
alls con	must be
be re programmed	must be
be re-programmed.	programmed
	more than once
Patent '363 Claim 27	Construction
A programmable	See claim 21
circuit as in	See claim 21.
claim 21	
wherein said means	See discussion of
for	"means for
programmably	programmably
connecting each	connecting" in
of said input leads of	claim 21 above Fach
or sure input loads of	

each of	of the
said configurable logic	"means for
	programmably
elements to at least	connecting" elements
one of	must
said interconnect	include pass
lines, said	transistors.
means for	
programmably	
connecting said at	
least one	
output lead of each of said	
configurable logic	
elements to	
at least one of said	
interconnect lines,	
said means	
for programmably	
connecting	
each of said	
input/output	
ports to at least one of said	
interconnect lines, and said	
means for	
programmably	
connecting each of	
said	
interconnect lines to	
at least	
one other of said	
interconnect	
lines comprise pass	
transistors.	
Patent '363 Claim 28	Construction
A programmable	See claim 27.
circuit as in	
claim 27	
wherein said means	See discussion of
for	"means for
programmably	programmably
connecting	connecting" in

further comprises	claims 21 and 27
memory	above. The
means, said memory	"memory means"
cells	element of this
forming at least part	claim has the same
of a	meaning as
shift register,	the "memory cells"
	element of
	claim 23. Each of the
	"means
	for programmably
	connecting"
	elements must include
	cells
	which are arranged to
	form at
	least part of a shift
	register.
wherein each of said	Each pass transistor
pass	must be
transistors is	controlled by one of
controlled by	the cells
one of said memory	which form part of the
cells, and	shift
	register.
wherein said means	See discussion of
for	"means for
programmably	programmably
connecting	connecting" in
further comprises	claims 21 and 27
means for	above. Each
transferring said series	of the "means for
of	programmably
signals through said	connecting" elements
shift	must
register until each of	include a structure
said	which is
signals is properly	the same as or the
located in	equivalent
an associated one of	of the structure in the
said	
memory cells	specification which
uniquely coupled	performs
to one of said pass	the function of
*	transferring a

transistors.	series of signals through the shift register until each signal is properly
	located in
	a cell which is only
	connected
	to one pass transistor. The
	structure disclosed in the
	specification is the clock
	signals (theta)1 and
	(theta)2 and pass
	transistors 53-1, 53-2,
	and
	53-3 of Figure 5. 6:52- 8:9
Patent '363 Claim 29	Construction
A programmable	See claim 28.
circuit as in	
claim 28	
in which said means	See discussion of
for	"means for
programmably	programmably
connecting	connecting" in
includes means for	claims 21, 27, and 28
changing	above.
the contents of said memory	Each of the "means for
cells, thereby to	programmably
reconfigure	connecting"
said programmable circuit.	elements must include a
	structure which is the
	same as
	or the equivalent of the
	structure disclosed in
	specification which
	the function of
	changing the
	und ing ing inc

	contents of the cells,
	thereby
	reconfiguring the
	programmable
	circuit. The structure
	disclosed in the
	specification
	is the dynamic shift
	register-static
	latch of Figure 5.
Patent '363 Claim 30	Construction
A programmable	A programmable
circuit	circuit is a
comprising:	circuit which is
e emprising.	capable of
	being programmed to
	perform
	different functions.
a plurality of logic	The circuit must have
elements,	more
each logic element	than one logic element.
having a	A
plurality of input leads	"logic element" is the
and	same as
at least one output	a "configurable logic
lead, and	
having a programming	element", defined in
means to	claim 11
cause said logic	above, 1:53-54. The
element to	input
perform a selected	leads, output leads, and
logic	11111, 111, 111, 111, 111, 111
function:	"programming means"
,	elements
	of this claim have the
	same
	meaning as the
	corresponding
	elements of claim 21.
a plurality of	The input/output ports.
input/output	1
ports;	interconnect lines, and
1 /	"means
	for programmably
	connecting"
	C

a group of interconnect elements of this claim lines; have the same meaning as the means for corresponding programmably elements of connecting each of claim 21. said input leads of each of said logic elements to at least one of said interconnect lines; means for programmably connecting said at least one output lead of each of said logic elements to at least one of said interconnect lines; means for programmably connecting each of said input/output ports to at least one of said interconnect lines; and means for programmably connecting each of said interconnect lines to at least one other of said interconnect lines;

whereby each of said logic	No construction necessary.
elements can be	5
programmed to	
perform a selected one	
of a	
plurality of logic	
functions,	
and said logic elements	
can be	
connected to each	
other and to	
said input/output ports	
ina	
selectable manner.	
Patent '363 Claim 31	Construction
A programmable	See claim 30.
circuit as in	
claim 30	
wherein programming	See discussion of
means of	"programming
each of said logic	means" in claims 21
elements	and 30
comprises transistors.	above. The
-	"programming
	means" element of each
	logic
	element must include
	transistors.
Patent '363 Claim 32	Construction
A programmable circuit	See claim 31.
as III claim 31	
wherein sold	See discussion of
nrogramming means	"programming
includes a plurality of	means" in claims 21
memory	30 and $311$ $111$ $1111$ $1111$ $1111$ $1111$
	31 above See
CEIIS	discussion of
	"memory coll" in claim
	23
	above. The
	"programming
	means" element must
	include

	more than one such
and wherein said	The transistors of claim
transistors	
are controlled by said	must be controlled by
are controlled by said	the
plurality of memory cel	lls. cells described above.
Patent '363 Claim 33	Construction
A programmable	See claim 32.
circuit as in	
claim 32	
in which said	The memory cells
plurality of	must be
memory cells forms	arranged so as to
at least	form at
part of a shift	least part of a shift
register,	1
	register. See Fig. 5.
control signals being	Control signals are
loaded	to be
into said memory	loaded into a shift
cells by	register
being transferred	by transferring
through said	(shifting)
shift register until	those signals from
each of	one cell to
said signals is	the next within the
properly	shift
located in said	register until the
corresponding	signals are
one of said memory	in their proper
cells.	locations.
Patent '363 Claim 34	Construction
A programmable	See claim 32.
circuit as in	
claim 32	
in which said memory	The memory cells
cells can	must be
be re-programmed.	capable of being
	programmed
	more than once.
Patent '363 Claim 36	Construction
A programmable	See claim 30.
circuit as in	,
claim 30	

wherein said means	See discussion of
nrogrammably	programmably
connecting	connecting" in
comprise transistors	claims 21 and 30
comprise transistors.	above Each
	"means for
	programmably
	connecting" element
	must
	include transistors.
Patent '363 Claim 37	Construction
A programmable	See claim 36.
circuit as in	
claim 36	
wherein said means	See discussion of
for	"means for
programmably	programmably
connecting	connecting" in
further comprise	claims 21, 30 and 36
memory cells,	above.
said memory cells	The memory cells
forming at	element of
least part of a shift	this claim has the
1	same
register.	meaning as the
	corresponding
	element of claim 23.
	Each of
	the "means for
	programmably
	connecting" elements
	must
	include cells which are
	arranged so as to form
	at
	least part of a shift
	register.
wherein said	The transistors must
transistors are	be
controlled by said	controlled by the cells
memory	-
cells, and	described above.
wherein said means	See discussion of

for	"means for
programmably	programmably
connecting	connecting" in
further comprises	claims 21, 30 and 36
means for	above.
transferring said series	Each "means for
of	programmably
signals through said shift	connecting" element
register until each of	include a structure
said	which is
signals is properly	the same as or the
located in	equivalent
an associated one of	of the structure in the
said	
memory cells.	specification which
•	performs
	the function of
	transferring a
	series of signals
	through the
	shift register until each
	signal is properly
	located in
	a cell. The structure
	disclosed in the
	specification
	is the clock signals
	(theta)1 and (theta)2
	and pass transistors
	53-1. 53-2.
	and 53-3 of Figure 5.
	6:52-8:9
Patent '363 Claim 38	Construction
A programmable	See claim 37.
circuit as in	
claim 37	
in which said means	See discussion of
for	"means for
programmably	programmably
connecting	connecting" in
includes means for	claims 21, 30, 36, and
changing	37
the contents of said	above. Each of the

memory	"means for
cells, thereby to	programmably
reconfigure	connecting"
said programmable	elements must include a
circuit.	
	structure which is the
	same as
	or the equivalent of the
	structure disclosed in
	the
	specification which
	performs
	the function of
	changing the
	contents of the cells.
	thereby
	reconfiguring the
	programmable
	circuit. The structure
	disclosed in the
	specification
	is the dynamic shift
	register-static
	latch of Figure 5.
Patent '363 Claim 57	Construction
A configurable logic	A CLA chip is a CLA
array	as defined
chip comprising:	in claim 11 above,
	implemented
	in a single integrated
	circuit.
a plurality of storage	A storage cell is a
cells	structure
for holding	that is capable of
configuration	retaining a
information, said	single bit of binary
	data.
configuration	6:31. The CLA chip
information	must have
configuring said	more than one storage
configurable	cell
logic array chip; and	which is able to retain
	configuration
	information for
	the CLA ship

	uie CLA cinp.
	Although the
	specification identifies
	а
	shift register-static
	latch as
	a particular type of
	storage
	cell that may be used,
	the
	structural language of this
	claim does not limit the
	type
	of storage cell that is
	claimed.
means for selecting	A structure which is the
Ø	same
configuration	as or the equivalent of
information from	the
a device external to	structure in the
said	specification
configurable logic	which performs the
array chip	function of
and initiating the	selecting configuration
transfer of	
said configuration	information from a
information	device
into said storage cells.	external to the CLA
	chip and
	initiating the transfer of
	that information to the
	storage cells described
	The structure disclosed
	in the
	specification is: standard
	circuitry that generates
	address signals and a
	control
	signal: ports to
	communicate
	those signals outside of
	the

	chip; and a port to
	receive
	configuration data from
	an
	external source. Fig.
	8B.
Patent '363 Claim 58	Construction
A configurable logic	See claim 57.
array	
chip as in claim 57	
in which said means	See discussion of
for	"means for
causing said	selecting
configuration	configuration
information to be	information and
loaded	initiating
causes said	transfer" in claim 57
configuration	above.
information to be	The "means for
loaded in	selecting
response to said	configuration
system being	information and
powered up.	initiating transfer"
	element
	must include a
	structure which
	is the same as or the
	equivalent of the
	structure in
	the specification
	which
	performs the function
	of
	causing the
	configuration
	information to be
	loaded in
	response to the
	system being
	powered up. The
	structure
	disclosed in the
	specification
	is: standard circuitry
	that

	generates address signals and a control signal; ports to communicate those signals outside of the chip; and a
	port to receive configuration data from an external source.
	11:43-12:22; Fig. 8B.
Patent '363 Claim 59	Construction
A configurable logic array	See claim 57.
chip as in claim 57	
in which said means	See discussion of
for	"means for
causing said	selecting
configuration	configuration
information to be loaded	information and initiating
causes said	transfer" in claim 57
configuration	above.
information to be	The "means for
loaded in	selecting
response to said	configuration
system being	information and
reset.	initiating transfer"
	element
	structure which
	is the same as or the
	aguivalant of the
	structure in
	the specification
	which
	performs the function of
	causing the configuration
	information to be
	loaded in
	regnance to the

	response to me
	system being
	reset. The structure
	disclosed in the
	specification
	is: standard circuitry
	that
	generates address
	signals and
	a control signal; ports
	to
	communicate those
	signals
	outside of the chip:
	and a
	port to receive
	configuration
	data from an external
	source.
	11:43-12:22: Fig. 8B.
Patent '363 Claim 81	Construction
A configurable system	A configurable system
0 5	is one
comprising:	or more devices
	connected
	together that can be
	configured to perform
	different functions.
one master	The master CLA
configurable logic	element of this
arrav:	claim has the same
	meaning as
	the corresponding
	element of
	claim 11.
at least one slave	The slave CLA
	element of this
configurable logic	claim has the same
array;	meaning as
<b>.</b> .	the corresponding
	element of
	claim 11. The system
	must
	include at least one
	slave

	CLA.
at least one memory:	The memory. "means
	for
said master	retrieving," "means for
configurable logic	0,
array having means for	using," and "means for
retrieving data from	passing" elements of
said at	this
least one memory,	claim have the same
	meaning as
means for first using	the corresponding
said	elements of
data for configuring	claim 11.
itself,	
and	
means for passing	
some of said	
data to said at least	
one	
slave configurable	
logic	
array.	7 Detent
Detent 1/487 Claim 1	/ Patent
A configurable logic	A configurable logic
arrav	arrav
comprising.	("CLA") is a circuit
comprising.	containing configurable
	logic
	elements which can be
	connected to each other
	and to
	inputs and outputs if
	any,
	through a configurable
	interconnect structure
	See
	in passim 1.54-58
a plurality of	A configurable logic
configurable	element
logic elements	("CLE") is "a
(CLEs),	combination of
(	
	devices which are

	being electrically
	interconnected by
	switches
	operated in response to
	control bits to
	[per]form any
	one of a plurality of
	logical
	functions." 1:14-18.
	The CLA
	must have more than
	one CLE.
each CLE having at	An input lead is a
least one	structure
input lead and at least	that can be used to
one	input a
output lead;	signal to a CLE. Each CLE
	must have at least one
	input
	lead. An output lead is
	a
	structure that can be used to
	output a signal from a CLE.
	Each CLE must have at least
	one output lead. See
	e.g.
	Figs. 2, 3A, 3B, 4A &
	7Ă.
a general interconnect	A general interconnect
structure comprising a	structure is defined
	using the
plurality of general	following definitions:
interconnect leads and	
a	
plurality of	Interconnect leads are
programmable	
general interconnect junctions	structures, regardless of
for interconnecting	their length, which
selected	conduct

ones of said general

interconnect leads;

data signals from place to place within the integrated circuit device. *See* Fig. 4A.

"The leads in Fig. 4A which are neither input leads nor output leads are all called general interconnect leads.. ..." 6:12-14.

Interconnect junctions are structures which connect one interconnect lead to another interconnect lead. *See* 1:64-66 and Fig. 4A.

"An access junction is a programmable junction for connecting a general interconnect lead to an input lead of a CLE or for connecting an output lead of a CLE to a general interconnect lead." 1:66-2:2.

"[T]he junctions in Fig. 4A which are not access

	junctions
	for input and output
	leads are
	called general
	interconnect
	junctions." 6:14-16.
	The general
	interconnect
	structure must have
	more than
	one general
	interconnect lead
	and more than one
	general
	interconnect junction.
one or more input	See discussion of
access	"access
junctions for each	junction" above. The
input lead,	CLA must
each of said input	have at least one input
access	access
junctions being	junction for each input
programmable	lead
for connecting a	of each CLE.
corresponding	
general interconnect	
lead to	
said input lead;	See diamonian of
one or more output	See discussion of
iunctions for each	aucos junction" above The
Junctions for each	CI A must
lead each of said	have at least one output
output	nave at reast one output
access junctions being	access junction for each
programmable for	output lead of each
connecting	CLE.
said output lead to a	
corresponding general	
interconnect leads	
means for	A structure which is the
nrogramming said	A SUBCLUIC WHICH IS THE
general interconnect	or the equivalent of
general interconnect	as of the equivalent of

iunctions	the
and said access	structure in the
iunctions to	specification
provide an electrical	which performs the
path	function of
connecting one of said	programming general
at	F
least one output lead	interconnect junctions
of one	and
of said plurality of	access junctions so as
CLEs to	to
one of said at least	provide an electrical
one input	path
lead of one of said	from an output lead of
plurality	one CLE
of CLEs, said	to the input lead of
electrical path	another
containing two access	CLE which contains
C	two access
junctions and at least	junctions and at least a
a	-
portion of one of said	portion of a general
general	
interconnect leads;	interconnect lead. The
and	
	structure disclosed in
	the
	specification is a
	memory, or
	a programming register.
	6:48-54,
	58-63. <i>See also</i> Figs. 3a
	and 3b (RAM) and Fig.
	5 (shift
	register (static latch)).
at least one special	A special
	interconnection is
interconnection circuit	one that connects an
which	output
permits a selected	lead of one CLE to the
output lead	input
of one of said CLEs	lead of another CLE,
to be	but that
connected to a	does not contain any
selected input	general

lead of another CLE, said	interconnect leads or any
special	junction in the general
interconnection	5 0 -
circuit not containing any	interconnect structure.
portion of the general	
interconnect leads or	As defined above
any	general
junction in the general	interconnect leads are all
interconnect structure.	leads except input leads and
	output leads. See above.
	The junctions that are in the
	general interconnect structure
	(referred to above as general
	interconnect junctions")
	those that are not access
	iunctions for input leads
	or
	output leads. See above.
	Therefore, access
	junctions
	that connect general
	interconnect leads to
	leads or output leads
	are not
	in the general
	interconnect
	structure.
Patent '487 Claim 3	Construction
A configurable logic	See claim 1.
array as	
in claim 1	
wherein said special	See discussion of
1	special
interconnection	interconnection

circuit	circuit in
comprises a lead	claim 1 above. The
connected to	special
said selected output	interconnection
lead and	circuit must
a pass transistor for	include: (1) a lead
each	connected
input lead of said	to a selected output
selected	lead of a
CLE connected	CLE ("the special
between said	lead"): and
lead composted to	(2) one need
lead connected to	(2) one pass
said	transistor
selected output lead	corresponding to
and said	each input
corresponding input	lead of another CLE.
lead.	Each
	pass transistor is
	able to
	connect between its
	corresponding input
	lead and
	the special lead.
The B1'479 Patent <sup>3</sup>	
Patent B1'479 Claim 1	Construction
A reprogrammable	A reprogrammable logic
logic array	array
device comprising:	device is a device that
de liee comprising.	can be
	programmed to perform
	various
	functions and that can be
	programmed more then
	once.
means forming a first	This is not a means-plus-
	function
programmable AND array	claim element. The
	datailed meritation of
	detailed recitation of
	structure included in this
	structure included in this claim language (see
	structure included in this claim language (see below) is
	structure included in this claim language (see below) is sufficient to rebut the
	structure included in this claim language (see below) is sufficient to rebut the
	presumption triggered by the
------------------------------	-------------------------------------
	use of the word "means." The
	claim language does not link
	the term "means" to any
	function, as "forming a first
	programmable AND array" fails
	to define a function. Rather,
	"forming a first
	programmable
	AND array" describes a
	structure. Therefore, this
	element is not construed
	according to s. 112 para. 6. The
	memory cells (described below)
	are arranged so as to form a
	programmable AND array, An
	AND array is more than one AND
	gate.
having a plurality of first	As this is a structural claim,
static, reprogrammable logic	the logic memory cells may be
memory cells	of any type as long as they
	are static and
	reprogrammable.
arranged in addressable rows	The memory cells are
and columns	physically arranged on the
	device in rows and
	columns.
	Each row must be
	addressable

	and each column must
	addressable
and which can be individually	The ability must exist to
programmed to contain logic	change the contents of one
data;	memory cell without changing
	the contents of any other
	cell. This phrase does not
	require the ability to
	program
	one memory cell at a
	time.
	11:24-27.
second static, reprogrammable	The second static,
architecture control	reprogrammable memory
memory	cells
cells, said second static	must be of the same type as
memory cells being of the same	the first static,
type as said first static	reprogrammable memory cells,
memory cells;	and there must be more than
	one of such cells.
first input circuit means for	A structure which is the same
receiving a first input signal	as or the equivalent of the
and for developing a	structure in the
first	specification
buffered signal	which performs the
corresponding	function of
thereto;	receiving a first input signal
	and developing a corresponding
	first buffered signal. The
	structure disclosed in the

	specification is the entire
	input circuit shown in
	Figure
	9.7:12-48.
first row driver means	A structure which is the same
responsive to said first	as or the equivalent of the
buffered signal and	structure in the
operative	specification
to interrogate a particular	which is responsive to the
row of said memory cells and	first buffered signal and
to cause said first AND array	which performs the function of
to output signals	interrogating a particular row
corresponding to the data	of memory cells and causing
contained therein;	the first AND array to output
	signals corresponding to the
	data contained therein. To
	interrogate means "to give or
	send out a signal to (as a
	transponder or computer) for
	triggering an appropriate
	response." Webster's New
	Collegiate Dictionary, 599
	(1981). The structure
	disclosed in the specification
	is the logic gates G11 and G12
	and the inverter formed
	by T13, T14 and T15 in

	Figure 10.
	7:49-8:2. The term
	"interrogate" does not
	require
	that the row driver apply
	a
	signal directly to the
	memory
	cells. Fig. 6A.
first sensing means for	A structure which is the same
sensing the signals	as or the equivalent of
output by	the
said first AND array	structure in the
and for	specification
developing a	which performs the
corresponding	function of
first data signal which	sensing the signals
is the	output by
logical OR of the signals	the first AND array and
output by said first	developing a
AND	corresponding
array;	first data signal which is
	the
	logical OR of the signals
	output by the first AND
	The structure disclosed
	in the
	specification is the OR/NOR
	Gate, Sense Amplifier of
	Figure 12. 8:31-55.
first signal storage	A structure which is the
means for	same
receiving and	as or the equivalent of
temporarily	the
storing said first data	structure in the
0	specification
signal;	which performs the
<i>U</i> ,	function of
	receiving and
	temporarily
	staring the first data

	storing the first data signal.
	The structure disclosed
	in the
	Flip-Flop
	of Figure 13. 8:56-9:8.
first output terminal	A structure which is the
means;	same
and	as or the equivalent of the
	structure in the
	specification
	which performs the
	function of
	providing an output on a
	terminal. The structure
	disclosed in the
	specification
	is the inverter formed by
	transistors P3 and N3,
	the
	inverter formed by P4 and N5,
	and the I/O pad, all of
	Figure
	16.9:57-10:11.
first switching means	A structure which is the
responsive to a control	same
signal	the
coupled to and	structure in the
responsive to	specification
contents of said second	which performs the
memory	tunction of
cells, said first	coupling either the first
switching	dala
couple	signal of a data signal
either said first data signal	temporarily stored in the
or a data signal	first signal storage means
temporarily	to
stored in said first signal	the first output terminal

storage means to said first	means in response to a control
output terminal means.	signal. The structure
	disclosed in the
	specification
	is the output multiplexer
	(OMUX) of Figure 14.
	9:9-44.

FN3. The Reexamination Certificate for this patent only includes those paragraphs of the specification affected by amendment. Therefore, citations to the specification for this patent refer to the specification of the original '479 patent unless otherwise noted. Patent B1'479 Claim 2. Construction

Patent B1479 Claim 2	Construction
A programmable logic	See claim 1.
array	
device as recited in claim	
1	
and further comprising	The device must
second	include a
row driver means	"second row driver
responsive to	means"
a signal input thereto	element. The "second
and	row
operative to	driver means" element
interrogate	of this
another particular row	claim is an additional
of said	
memory cells and to	structure which has
cause said	the same
first AND array to	meaning as the "first
output	row
other data signals	driver means" element
	of claim
corresponding to the	1. The "second row
data	driver
contained therein to	means" element must
said	
first sensing means for	interrogate a different
	row of
developing another	memory cells than the
data	"first
signal.	row driver means"
	element so
	as to output another
	data
	gianal to the "first

	signal to the first
	sensing
	means" element.
Patent B1'479 Claim 5	Construction
A programmable	See claim 2.
logic array	
device as recited in	
claim 2	
wherein said first switching	See discussion of "first
means is also	switching means" in
operative to	claim 1
couple either the	above. A structure
data signal	which is
output by said first	the same as or the
sensing	equivalent
means or a data signal	of the structure in the
temporarily stored	specification which
in said	performs
first signal storage	the function of the
means	"first
into said second row	switching means"
driver	above, and,
means.	in addition, the function
	of
	coupling either the data
	signal output by the
	first
	sensing means or a data signal
	temporarily stored in
	the
	first signal storage
	means
	into the second row
	driver
	means. The structure
	disclosed in the
	specification
	is the OMUX of Figure
	14 and
	the feedback
	multiplexer
	("FMUX") of Figure
	( I WIGA ) OF Figure

	15.9:9-19,
	45-56.
Patent B1'479 Claim 6	Construction
A programmable	See claim 5.
logic array	
device as recited in	
claim 5	
wherein said first	See discussion of
switching	"first
means includes an	switching means" in
output	claims 1
multiplexing device	and 5 above. The "first
for	
connecting either the	switching means"
output	element must
of said first sensing	include an output
means or	multiplexing
the temporarily	device.
stored first	
data signal contained	
in said	
first storage means to	
said	
first output terminal	
means.	
Patent B1'479 Claim 7	Construction
A programmable	See claim 6.
logic array	
device as recited in	
claim 6	
wherein said first	See discussion of
switching	"IIISU
means further	switching means" in
includes a	claims I,
teedback	5 and 6 above. The
multiplexing circuit	
operative to couple	switching means"
either the	element must
output of said first	include a feedback
sensing	
means, the	multiplexing circuit.
first data size 1	
the data	
une uata	

appearing at salu mist	
terminal means to	
said second	
row driver means.	
Patent B1'479 Claim 19	Construction
A programmable logic	See claim 1.
array	
device as recited in	
claim 1	
and further comprising:	
means forming a second	The "second
-	programmable AND
programmable AND	array", "second input
array having	circuit
a plurality of memory	means", "second row
cells	driver
arranged in addressable	means", "second sensing
rows	
and columns and which	means", "second signal
can be	storage
individually	means", "second output
programmed to	
contain logic data;	terminal means", and "second
second input circuit	switching means"
means for	elements of
receiving a second input	this claim all have the same
signal and for	meaning as the
developing a	corresponding
second buffered signal	elements of claim 1 The
corresponding thereto:	device must include a
corresponding increto,	second
second row driver	one of each of these
means	elements.
responsive to said	
second	
buffered signal and	
operative	
to interrogate a first	
particular row of said	
second	
AND array memory	
cells and to	

cause said second AND array to output signals corresponding to the data contained therein: second sensing means for sensing the signals output by said second AND array and for developing a corresponding second data signal which is the logical OR of the signals output by said second AND array; second signal storage means for receiving and temporarily storing said second data signal; second output terminal means; and second switching means responsive to a control signal and operative to couple either said second data signal or a data signal temporarily stored in said second signal storage means to said second output terminal means.

Patent B1'479 Claim 20	Construction
A programmable logic	See claim 19.
array	
device as recited in clair	n
19	
and further comprising	The device must
third	include a
row driver means	"third row driver
responsive to	means"
a signal input thereto and	element. The "third row
operative to	driver means" element
interrogate	of this
another particular row of said	claim is an additional
memory cells in said second	structure which has the same
AND array and to cause said	meaning as the "first row
second AND array to	driver means" element
output	of claim
other data signals	1 The "third row driver
corresponding to the data	means" element must
contained therein to said	interrogate a different row of
second sensing means for	memory cells in the second AND
developing another data	array than the "second row
signal.	driver means" element
	output another data
	signal w
	me second sensing means"
	element
Patent B1'479 Claim	Construction
21	
A programmable S logic array	See claim 20.
device as recited in claim 20	
wherein said first	See discussion of
switching '	'first

means is also	switching means" in
operative to	
couple either the	above. A structure
data signal	which is
output by said first	the same as or the
sensing	equivalent
means or a data	of the structure in the
signal	an a sifi action which
in said	specification which
first signal storage	the function of the
means	"first
into said third row	switching means"
driver	element
means.	above and in
	addition, the
	function of coupling
	either
	the output of the first
	sensing means or a
	data signal
	temporarily stored in
	the
	first signal storage
	means to
	the third row driver
	means.
	The structure
	disclosed in the
	Specification is the
	Figure 1/ and the
	FIGURE 14 and the
	Figure 15
Patent B1'479 Claim 3	6 Construction
A reprogrammable log	ic A reprogrammable logic
array	array
device comprising:	device is a device that
	can be
	programmed to perform
	various
	functions and that can be
	programmed more than
	once.

The "first programmable

	AND
means forming a first	array" element of this claim
programmable AND	has the same meaning as
array having	the
a plurality of static,	corresponding element of claim
reprogrammable logic	1.
memory	
cells arranged in	
addressable	
rows and columns and	
which can	
be individually	
programmed to	
contain logic data;	
a static programmable	The device must include
1 0	а
architecture control	static programmable
memory	······ · · · · · · · · · · · · · · · ·
cell;	architecture control
,	memory
	cell.
first input circuit means	cell. The "first input circuit
first input circuit means for	cell. The "first input circuit
first input circuit means for receiving a first input	cell. The "first input circuit means", "first row driver
first input circuit means for receiving a first input signal	cell. The "first input circuit means", "first row driver
first input circuit means for receiving a first input signal and for developing a	cell. The "first input circuit means", "first row driver means", and "first
first input circuit means for receiving a first input signal and for developing a first	cell. The "first input circuit means", "first row driver means", and "first sensing
first input circuit means for receiving a first input signal and for developing a first buffered signal	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto;	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto;	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative to interrogate a	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative to interrogate a particular	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative to interrogate a particular row of said memory	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative to interrogate a particular row of said memory cells and	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative to interrogate a particular row of said memory cells and to cause said first AND	cell. The "first input circuit means", "first row driver means", and "first sensing means" elements of this claim all have the same meaning as the corresponding elements of claim 1.

to output signals	
corresponding to the	
data	
contained therein;	
first sensing means for	
sensing the signals	
output by	
said first AND array and	
for	
developing a	
corresponding	
first data signal which is	
the	
logical OR of the	
signals	
output by said first AND	
array;	
first signal storage	A structure which is the
means for	same
receiving and	as or the equivalent of
temporarily	the
storing said first data	structure in the
	specification
signal, operation of said	which performs the
signal storage means	receiving and
signal storage means	temporarily
controlled by at least a	storing a first data signal
first	storing a mist data signal
control signal said first	and which is controlled
control signal, sald first	by a
control signal derived	first control signal. The
from at	
least one of said input	control signal must be
1	derived
signals based on	from at least one input
contents of	signal
at least one signal	based on the contents of
storage	at
memory cell, said signal	least one static
storage memory cell	reprogrammable memory
being a	cell.
static, reprogrammable	The structure disclosed in
memory	the

cell;	specification is the D Flip-Flop
	of Figure 13. Control
	signals are portrayed in
	Figure 13 as SET-bar.
	RESET-bar,
	CLK, and CLK-bar.
first output terminal	The "first output terminal
means;	•
and	means" and "first
	switching
first switching means	means" elements of this claim
responsive to a second	have the same meaning
control	as the
signal coupled to and	corresponding elements
	of
responsive to contents of said	claim 1.
architecture control	
memory	
cell, said first switching	
means operative to	
couple	
either said first data	
signal	
or a data signal	
temporarily	
stored in said first signa	1
storage means to said	
first	
output terminal means.	
Patent B1'479 Claim 37	Construction
A programmable	See claim 36.
logic array	
device as recited in	
$\frac{\text{claim 36}}{1 \cdot 1 \cdot 1}$	
wherein said signal	See discussion of
magna is a D flin	signal
flop having	storage means" in
a resot signal line	above The "signal
a reset signal line	storage
said first control	means" element
salu III si control	means ciement

signal.	must be a D
8	Flip-Flop which has
	a reset
	signal line coupled
	to the
	first control signal.
Patent B1'479 Claim	Construction
38	
A programmable	See claim 37.
logic array	
device as recited in	
claim 37	
wherein said first	The first control
control	signal must
signal is a logical	be either an
function	inverted,
of at least one of	buffered input
said	signal or a
inputs, said logical	non-inverted,
function	buffered input
selected from the	signal.
group	C
consisting of	
invereting	
[sic], or non-	
inverting	
buffered.	
Patent B1'479 Claim 39	Construction
A programmable	See claim 37.
logic array	
device as recited in	
claim 37	
wherein a clock	The "signal storage
input to said	means"
signal storage means	element must
is	include a clock
coupled to one of	input that is
said input	connected to one
signals.	of the input signals.
Patent B1'479 Claim 40	Construction
A programmable	See claim 37.
logic array	
device as recited in	
claim 37	
wherein a clock	The D Flip-Flop must

input to said	include a
flip flop is coupled	clock input that is
to one of	connected
said input signals.	to one of the input
	signals.
Patent B1'479 Claim	Construction
41	
A programmable	See claim 36.
logic array	
device as recited in	
claim 36	
wherein said output	See discussion of
terminal	"output
means comprises an	terminal means" in
output	claim 36
circuit that	above. The "output
selectively	terminal
couples logic output	means" element must
to an	include an
output pin, said	output circuit that either
output	• • • • • • • • • • • • • • • • • • •
circuit coupled to	connects or does not
and	connect
controlled by a	the logic output to an
product term	output
from said AND	nin A product term
arrav.	from the
5	AND array must be
	connected to
	the output circuit and
	determine whether the
	circuit
	connects or does not
	connect
	the logic output to an
	output
	pin.
Patent B1'479 Claim 42	2Construction
A programmable	See claim 36.
logic array	
device as recited in	
claim 36	
wherein said output	See discussion of
terminal	"output
means is adapted to	terminal means" in

	claim 36
alternately receive	above. A structure
input from	which is
an input/output pin.	the same as or the
	equivalent
	of the structure in the
	specification which
	performs
	the function of the
	"output
	terminal means"
	above, and, in
	addition. alternately
	receives
	input from an
	input/output
	pin. The structure
	disclosed
	in the specification is
	all of
	Figure 16, except the
	"Input
	Circuit (Fig.9)".
Patent B1'479 Claim 43	Construction
A programmable	See claim 36.
logic array	
device as recited in	
claim 36	
further comprising a	The device must
feedback	include a
circuit adapted to	feedback circuit that
selectively	18
feed back to an AND	capable of
input	connecting either
either said first data	the first data signal
sıgnal	or the
or said data signal	temporarily stored
· · · · ·	data signal
temporarily stored.	to an AND input.
Patent B1'479 Claim 48	Construction
A programmable logic	A programmable logic
array	array
device comprising:	device is a device that
	nrammad ta

	perform various
	functions.
means forming a first	The "first
means forming a first	programmable AND
programmable AND	array" element of this
array having	claim
a plurality of logic	has the same meaning
memory	as the
cells arranged in	corresponding element
addressable	of claim
rows and columns and	1 with the following
which can	1 with the following
be individually	exception: the AND
programmed to	array has
contain logic data;	memory cells that are
	described as "logic
	memory
	cells" rather than "first
	static reprogrammable
	logic
	memory cells." The
	memory
	cells in this claim do
	not
	need to be
	reprogrammable or
	static.
first input circuit means for	The "first input circuit
receiving a first input	means". "first row
signal	driver
and for developing a	means". "first sensing
first	means",
buffered signal	"first signal storage
corresponding	means",
thereto;	and "first output
,	terminal
first row driver means	means" elements of
	this claim
responsive to said first	all have the same
1	meanings as
buffered signal and	the corresponding
operative	elements of
to interrogate a	claim 1
to monogate a	

particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein; first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array; first signal storage means for receiving and temporarily storing said first data signal; first output terminal means; second row driver The structure corresponding to means the "second row driver responsive to a signal means" input thereto and operative to element of this claim has the interrogate another same meaning as the particular row of said memory corresponding element

of claim

2.

cells and

array

signals

to cause said first AND

to output other data

corresponding to the

corresponding to the data	
contained therein to said	
first sensing means for	
developing another data	
signal and	
first switching means	$\Delta$ structure which is
mist switching means	the same
responsive to a control	as or the equivalent of
signal	the
and operative to couple either	structure in the specification
said first data signal or a	which performs the function of
data signal temporarily stored	connecting either the first
in said first signal storage	data signal or a data signal
means to said first	temporarily stored in
output terminal maans and also	une
terminal means and also	to the
operative to couple either the	output terminal means, and
data signal output by	also connecting either
first sensing means or a	same first data signal
data	or that
signal temporarily	same data signal
stored in	temporarily
said first signal storage	stored in the signal storage
means into said second	means to the second
row	row driver
driver means, said first	means. The structure
switching means further	disclosed in the
	specification
comprising:	is the OMUX of
	Figure 14 and
	15.
i) an output	The first switching
multiplexing	means must
device for connecting either	include a multiplexing device

the output of said first	that connects either a data
sensing means or the	signal from the sensing means
temporarily stored first data	or a data signal temporarily
signal contained in said	stored in the signal
first	storage
signal storage means to	means to the output
said	terminal
first output terminal	means.
means;	
and	
ii) a feedback	The first switching
multiplexing	means must
circuit operative to	include a feedback
couple	
either the output of said	that
first sensing means, the	connects either a data signal
temporarily stored first	from the sensing
data	means, a data
signal, or the data	signal temporarily
appearing	stored in
at said first output	the signal storage
terminal	means, or
means to said second	the data signal that
row	appears
driver means.	at the output terminal means
	to the second row
	driver
	means.
Patent B1'479 Claim 49	Construction
A programmable logic	See claim 48.
device as	
recited in claim 48	
wherein said feedback	See discussion of feedback
multiplexing circuit is	multiplexing circuit in claim
adapted to feed back a	48 above. The
*	feedback
selected signal to logic	multiplexing circuit

	must be
inputs without	able to connect a
applying said	selected
selected signal to an	signal to the second
output	row
pin of said	driver means
programmable logic	without
device.	connecting that
	signal to an
	output pin.
Patent B1'479 Claim 55	Construction
A reprogrammable logic	A reprogrammable
array	logic array
device comprising:	device is a device that
	can be
	programmed to perform
	various
	functions and that can
	be
	programmed more than
	once.
means forming a first	The "first
	programmable AND
programmable AND	array" element of this
array having	claim
a plurality of logic	has the same meaning
memory	as the
cells arranged in	corresponding element
addressable	of claim
rows and columns and	48.
which can	
be individually	
programmed to	
contain logic data,	
wherein each of said	The first programmable
plurality	AND
of memory cells	array must have
comprise first	memory cells
and second MOS	made up of two MOS
transistors	transistors
coupled in series	connected in series.
between	One of
first and second nodes,	the transistors must
one of	include a
said first or second	gate that holds an

	electrical
transistors comprising a	charge for a substantial
gate	
having a substantial	length of time. The
time-invariant	-
charge thereon based	electrical charge must be
on a programming input,	based on a programming input.
whereby said first and second	The two transistors must
transistors cooperate to	cooperate to produce a logic
produce said logic cell data	signal at an output node.
at an output node;	
first input circuit means for	The "first input circuit
receiving a first input	means", "first row
signal	driver
and for developing a	means", "first sensing
first	means",
buffered signal	"first signal storage
corresponding	means",
thereto;	and "first output terminal
first row driver means	means" elements of this claim
responsive to said first	have the same meanings as the
buffered signal and	corresponding elements
operative	of
to interrogate a particular	claim 1.
row of said memory cells and	
to cause said first AND array	
to output signals	
corresponding to the data	
continued therein based	
said logic cell data;	

first sensing means for	
sensing the signals	
output by	
said first AND array and	
for	
developing a	
corresponding	
first data signal which is	
the	
logical OR of the	
signals	
output by said first AND	
array;	
first signal storage	
means for	
receiving and	
temporarily	
storing said first data	
signal;	
first output terminal	
means;	
and	
first switching means	A structure which is the
	same
responsive to a control	as or the equivalent of
signal	the
and operative to couple	structure in the
eitner	specification
said first data signal or a	which performs the function of
	iunction of
data signal temporarily stored	connecting either a data
in said first signal	signal from the sensing
storage	means
means to said first	or a data signal
output	temporarily
terminal means.	stored in the signal
	storage
	means to the output terminal
	means in response to a control
	signal The structure

disclosed in the

specificationis the OMUX of Figure14.Patent B1'479 Claim 57ConstructionA reprogrammable logicA reprogrammablearraylogic arraydevice for operation in adevice is a device that can belogic systemprogrammed tocomprising:perform various functions and that can bemeans forming a firstThe "first programmable AND array" element of this array having claima plurality of logichas the same meaning memory as thecells arranged in addressablecorresponding element datasof claimcorresponding element of claimindividually programmed to contain logic data;The "first input circuit means", "first row driver and for developing a firstfirst input circuit means for receiving a firstThe "first signal storage means", "first soutput terminal means", and "first output terminalfirst row driver means"first output terminal		uisciosca ili uic	
is the OMUX of Figure 14.Patent B1'479 Claim 57ConstructionA reprogrammable logic arrayA reprogrammable logic array device for operation in a device is a device that can belogic system comprising:programmed to perform various functions and that can bemeans forming a first array having a plurality of logic memoryThe "first programmable AND array" element of this claima plurality of logic memoryhas the same meaning as the corresponding element of claimof claim rows and columns and thich can be individually programmed to contain logic data;The "first input circuit first input circuit means for receiving a first input signalfirst input circuit means for receiving a first input signalThe "first signal storage means", "first soutput terminal means", and "first output terminal means", and "first output terminal means", elements of		specification	
Patent B1'479 Claim 57ConstructionA reprogrammable logic arrayA reprogrammable logic arraydevice for operation in a comprising:device is a device that can belogic system comprising:programmed to perform various functions and that can bemeans forming a firstThe "first programmable AND array" element of this array having a plurality of logic news and columns and which can be individually programmed to contain logic data;first input circuit means for receiving a first input after the individually means", "first sensing means", "first sensing first signal storage means", "first soutput terminal first signal storage means", "first output terminal first soutput terminal first soutput terminal first row driver means		is the OMUX of Figure 14.	
A reprogrammable logic arrayA reprogrammable logic array device for operation in a device is a device that can belogic system comprising:programmed to perform various functions and that can bemeans forming a first array having a plurality of logic memoryThe "first programmable AND array" element of this array " element of this calim a s the corresponding element of claimaddressable of claimof claim receiving a first input circuit means for claimrows and columns and which can be individually programmed to contain logic data; first input circuit means for receiving a first input signalThe "first input circuit first signal storage means", "first sensing first signal storage corresponding driver and for developing a first signal storage corresponding thereto; and "first output terminal first row driver means	Patent B1'479 Claim 57	Construction	
arraylogic arraydevice for operation in adevice is a device that can belogic systemprogrammed to perform various functions and that can bemeans forming a firstThe "first programmable AND array" element of this array having a plurality of logic memorya plurality of logic memoryhas the same meaning as the corresponding element of claimaddressable of claimof claimrows and columns and which can be individually programmed to contain logic data;The "first input circuit for receiving a first input means", "first sensing firstfirst input circuit means for receiving a first input signalThe "first signal storage means", "first output terminal means", elements of	A reprogrammable logic	A reprogrammable	
device for operation in a logic systemdevice is a device that can belogic systemprogrammed to perform various functions and that can bemeans forming a firstThe "first programmable AND array" element of this caim a plurality of logic memorya plurality of logic memoryhas the same meaning as the corresponding element of claimaddressable vontain logic data;of claim first input circuit means for receiving a first input signalfirst input circuit means firstThe "first sensing means", "first sensing first signal storage correspondingfirst row driver means", and "first output terminal first row driver meansmeans", elements of	array	logic array	
logic system comprising:programmed to perform various functions and that can bemeans forming a firstThe "first programmable AND array" element of this claim a plurality of logic memorya plurality of logic memoryhas the same meaning as the corresponding element of claimcells arranged in addressablecorresponding element of claimbe individually programmed to contain logic data;The "first input circuit first input circuit means means", "first row driver and for developing a firstfirstmeans", "first sensing means", "first sensing first output terminal means", and "first output terminal first row driver means	device for operation in a	device is a device that can be	
comprising:perform various functions and that can bemeans forming a firstprogrammed more than once.means forming a firstThe "first 	logic system	programmed to	
IIIfunctions and that can beprogrammed more than once.means forming a firstThe "first programmable AND array" element of this array having a plurality of logic memorya plurality of logic memoryhas the same meaning as the corresponding element of claimaddressable which can be individually programmed to contain logic data;corresponding element of claimfirst input circuit means for receiving a first input signalThe "first input circuit first sensing means", "first sensing first signal storage correspondingfirst row driver means"first output terminal means", elements of	comprising:	perform various	
Decprogrammed more than once.means forming a firstThe "first programmable AND array" element of this array having a plurality of logic memorya plurality of logic memoryhas the same meaning memory as the corresponding element addressablecells arranged in addressablecorresponding element of claimrows and columns and which can be individually programmed to contain logic data;Kenter first input circuit means for receiving a first input signalfirst input circuit means firstThe "first input circuit first sensing means", "first sensing first signal storage correspondingfirst row driver meansmeans", and "first output terminal first row driver means	r C	functions and that can	
programmed more man once.means forming a firstThe "first programmable AND array" element of this array havinga plurality of logic memoryhas the same meaning as the corresponding element of claimaddressableof claim of claimrows and columns and which can be individually programmed to contain logic data;Means", "first input circuit first input circuit means driverfirst input circuit means firstThe "first input circuit means", "first row signaland for developing a firstmeans", "first sensing means", "first sensing first signal storage correspondingfirst row driver meansmeans", and "first output terminal means", elements of		programmed more than	
means forming a firstThe "first programmable AND array" element of this array having a plurality of logic memoryarray" element of this claim as the same meaning memory as the cells arranged in addressablecells arranged in addressablecorresponding element of claimrows and columns and be individually programmed to48.contain logic data; first input circuit means for receiving a first input signalThe "first input circuit first sensing means", "first sensing first signal storage correspondingfirst row driver means"first output terminal means", elements of		once.	
programmable AND array havingprogrammable AND array" element of this claima plurality of logic memoryhas the same meaning as thecells arranged in addressablecorresponding element of claimaddressableof claimrows and columns and which can48.be individually programmed toThe "first input circuit forreceiving a first input signalmeans", "first row driverand for developing a firstmeans", "first sensing means", "first sensing means", "first signal storage correspondingfirst row driver meansmeans", elements of	means forming a first	The "first	
programmable AND array havingarray" element of this claima plurality of logic memoryhas the same meaning as thecells arranged in addressablecorresponding element of claimaddressableof claimrows and columns and be individually programmed to48.contain logic data;	-	programmable AND	
array havingclaima plurality of logichas the same meaninga plurality of logichas the same meaningas thecorresponding elementaddressableof claimrows and columns and48.which canbe individuallyprogrammed tocontain logic data;first input circuit meansThe "first input circuitforreceiving a first inputreceiving a first inputmeans", "first rowsignaldriverand for developing ameans", "first sensingfirstmeans", "first signal storagecorrespondingmeans",thereto;and "first outputterminalfirst output	programmable AND	array" element of this	
a plurality of logichas the same meaning as thememoryas thecells arranged in addressablecorresponding element of claimaddressableof claimrows and columns and which can48.which canbe individually programmed tocontain logic data;	array having	claim	
memoryas thecells arranged in addressablecorresponding element of claimaddressableof claimrows and columns and which can48.which can be individually programmed to48.contain logic data;	a plurality of logic	has the same meaning	
cells arranged in addressablecorresponding element of claimaddressableof claimrows and columns and which can48.which canbe individually programmed tocontain logic data;	memory	as the	
addressableof claimrows and columns and48.which can48.be individuallyprogrammed tocontain logic data;	cells arranged in	corresponding element	
rows and columns and which can be individually programmed to48.contain logic data;	addressable	of claim	
which can be individually programmed to contain logic data; first input circuit means for receiving a first input signal driver and for developing a means", "first row first means", "first sensing first means", "first sensing means", "first signal storage corresponding means", thereto; thereto; and "first output terminal first row driver means means" elements of	rows and columns and	48.	
be individually programmed to contain logic data; first input circuit means for receiving a first input signal driver and for developing a means", "first sensing first means", "first sensing means", "first sensing means", "first sensing first means", "first sensing first means", "first sensing first means", "first sensing first signal storage corresponding means", thereto; and "first output terminal first row driver means means" elements of	which can		
programmed tocontain logic data;first input circuit meansforreceiving a first inputmeans", "first rowsignaldriverand for developing afirstmeans", "first sensingfirstbuffered signalcorrespondingmeans",thereto;and "first outputthereto;and "first outputterminalfirst row driver meansmeans" elements of	be individually		
contain logic data;first input circuit meansThe "first input circuitforThe "first input circuitformeans", "first rowsignaldriverand for developing ameans", "first sensingfirstmeans", "first sensingfirstmeans", "first sensingcorrespondingmeans",thereto;and "first outputfirst row driver meansmeans" elements of	programmed to		
first input circuit meansThe "first input circuitforreceiving a first inputmeans", "first rowsignaldriverand for developing ameans", "first sensingfirstmeans", "first sensingcorresponding"first signal storagecorrespondingmeans",thereto;and "first outputfirst row driver meansmeans" elements of	contain logic data;		
receiving a first input means", "first row driver and for developing a means", "first sensing first means", "first sensing means", "buffered signal means", "first signal storage corresponding means", thereto; and "first output terminal first row driver means means" elements of	first input circuit means for	The "first input circuit	
signaldriverand for developing ameans", "first sensingfirstmeans",buffered signal"first signal storagecorrespondingmeans",thereto;and "first outputfirst row driver meansmeans" elements of	receiving a first input	means", "first row	
and for developing a firstmeans", "first sensing means",buffered signal corresponding"first signal storage means",thereto;and "first output terminalfirst row driver meansmeans" elements of	signal	driver	
firstmeans",buffered signal"first signal storagecorrespondingmeans",thereto;and "first outputfirst row driver meansmeans" elements of	and for developing a	means", "first sensing	
buffered signal"first signal storagecorrespondingmeans",thereto;and "first outputterminalterminalfirst row driver meansmeans" elements of	first	means",	
correspondingmeans",thereto;and "first output terminalfirst row driver meansmeans" elements of	buffered signal	"first signal storage	
thereto; and "first output terminal first row driver means means" elements of	corresponding	means",	
terminal first row driver means means" elements of	thereto;	and "first output	
first row driver means means" elements of	,	terminal	
this claim	first row driver means	means" elements of this claim	
responsive to said first have the same	responsive to said first	have the same	
meanings as the	100 point v to build mot	meanings as the	
buffered signal and corresponding	buffered signal and	corresponding	
operative elements of	operative	elements of	
to interrogate to a claim 1.	to interrogate to a	claim 1.	

particular	
row of said memory	
cells and	
to cause said first AND	
array	
to output signals	
corresponding to the	
data	
contained therein;	
first sensing means for	
sensing the signals	
output by	
said first AND array and	
for	
developing a	
corresponding	
first data signal which is	
the	
logical OR of the	
signals	
output by said first AND	
array;	
first signal storage	
means for	
receiving and	
temporarily	
storing said first data	
signal;	
first output terminal means	•
first switching means	The "first switching means"
responsive to a control	element of this claim
signal	has the
and operative to couple	same meaning as the
either	8
said first data signal or a	corresponding element
C	of claim
data signal temporarily	55.
stored	
in said first signal	
storage	
means to said first	
output	1
terminal means;	

and means in said	A structure which is
system for	the same
modifying a	as or the equivalent of
programmed state	the
of selected memory	structure in the
cells in	specification
real time based on	which performs the
conditions, whereby	modifying a
salu	programmed state
programmable logic	of selected memory
allay is	real time based on
adaptive to sald system.	selected
	conditions The
	structure
	disclosed in the
	specification
	is the programming
	circuitry
	portraved in Figures
	17, 18,
	19, 20, 21, 22A and
	22B.
	10:20-15:7.
Patent B1'479 Claim 58	Construction
A reprogrammable logic	A reprogrammable
array	logic array
device comprising:	device is a device that
	can be
	programmed to
	perform various
	functions and that can
	be
	programmed more than
	once.
means forming a first	The "first
	programmable AND
programmable AND	array" element of this
array having	claim
a plurality of logic first	has the same meaning
	as the
reprogrammable	corresponding element
memory cells	ot claim
arranged in addressable	1 with the following

rows	
and columns and which	exception: the AND
can be	array has
individually	memory cells that are
programmed to	
contain logic data;	described as "logic first
	reprogrammable
	memory cells"
	rather than "first static
	reprogrammable logic
	memory
	cells." The memory
	cells in
	this claim do not need
	to be
	static.
second reprogrammable	The second
	reprogrammable
architecture control	memory cells must
memory	control the
cells;	routing of signals
	through the
<u> </u>	device. 9:22-25, 51-54.
first input circuit means	A structure which is
101 reactiving at least first	as or the equivalent of
and	the
second input signals	structure in the
trom	specification
respective first and	which performs the
second	function of
input pins, and for	receiving at least first
developing	and
bullered signals	second input signals
thereter	first and second input
unereto;	ning
	pills and developing
	corresponding
	buffered signals. The
	atmoture disclosed in
	the
	specification is the

	entire
	input circuit shown in
	Figure
	9.7:12-48.
first row driver means	A structure which is
	the same
responsive to said	as or the equivalent of
buffered	the
signals and operative to	structure in the
	specification
interrogate a particular	which is responsive to
row	the
of said memory cells	first and second
and to	buttered
cause said first AND	signals and which
array to	performs the
output signals	tunction of
corresponding	interrogating a
to the data contained	particular row of the
therein;	memory
	cells and causing the
	11fSt
	AND array to output
	signals
	dota
	uala
	interrogate means "to
	give or
	send out a signal to (as
	a turu an an dan an
	transponder or
	triagoning on
	unggernig an
	appropriate response "Wabster's
	New
	Collegiate Dictionary, 599
	(1981). The structure
	disclosed in the
	specification
	is the logic gates G11
	and G12
	and the inverter

	and the inverter formed by T13, T14 and T15 in Figure 10. 7:49-8:2. The term "interrogate" does not require that the row driver apply a signal directly to the memory
	cells. Fig. 6A.
first sensing means for	This element has the same
sensing the signals	meaning as the
output by	corresponding
said first AND array and	element of claim 1
tor	above.
developing a	
corresponding	
Tirst data signal which is	
logical OD of the	
signals	
output by said first $\Delta ND$	
output by salu IIIst AND	
first signal storage	A structure which is
means for	the same
receiving and	as or the equivalent of
temporarily	the
storing said first signal	structure in the
storing sala mot signal,	specification
said first signal storage	which performs the
	function of
means comprising a	receiving and
clock	temporarily
input, said clock input	storing the first data
coupled to said first	The structure disclosed
input	in the
pin;	specification is the D
1 ′	Flip-Flop
	of Figure 13. 8:56-9:8.
	The "first signal
	storage

	means" element must
	include a
	clock input which is
	connected
	to the first input pin of
	the
	input circuit means.
first output terminal	The "first output
means:	terminal
and	means" and "first
	switching
first switching means	means" elements of
	this claim
responsive to a control	have the same
signal	meanings as the
coupled to and	corresponding
responsive to	elements of
contents of said second	claim 1.
memory	
cells, said first	
switching	
means operative to	
couple	
either said first data	
signal	
or a data signal	
temporarily	
stored in said first signal	
storage means to said	
first	
output terminal means.	
Patent B1'479 Claim 59	Construction
A programmable logic	A programmable logic
array	array
device comprising:	device is a device that
	can be
	programmed to
	perform various
	functions.
means forming a first	The "first
~	programmable AND
programmable AND	array" element of this
array having	claim
a plurality of first logic	has the same meaning
	as the

reprogrammable	corresponding element
memory cells	of claim
arranged in addressable	58.
rows	
and columns and which	
can be	
individually	
programmed to	
contain logic data;	
second reprogrammable	The second
	reprogrammable
architecture control	architecture control
memory	memory
cells, said second	cells must control the
memory	routing
cells comprising at least	of signals through the
а	device.
storage selection	9:22-25, 51-54. The
memory cell,	second
a feedback control	set of memory cells
memory	must
cell, and an output	include at least a
control	storage
memory cell;	selection memory cell,
	a
	feedback control
	memory cell,
	and an output control
	memory
	cell.
	A storage selection
	memory
	cell contains data that
	determines whether to
	supply a
	data signal from the
	sensing
	means or a temporarily
	stored
	data signal to the
	output
	terminal means. See
	discussion of "first

	switching
	means" below.
	A feedback control
	memory cell
	contains data that
	determines
	whether or not to
	supply a
	data signal from the
	sensing
	means to the AND
	array. See
	discussion of
	"feedback
	switching means"
	below.
	An output control
	memory cell
	contains data that
	determines
	whether or not to
	supply an
	output signal to an
	pin See discussion of
	"first
	output terminal means"
	below.
first input circuit means	The "first input circuit
for	Ĩ
receiving a first input	means", "first row
signal	driver
and for developing a	means", "first sensing
first	means",
buffered signal	and "first signal
corresponding	storage
thereto;	means" elements of
	this claim
first row driver means	have the same
	meanings as the
responsive to said first	corresponding
_	elements of

buffered signal and claim 1. operative to interrogate a particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein; first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array; first signal storage means for receiving and temporarily storing said first data signal; first output terminal A structure which is the same means, said output terminal as or the equivalent of means the comprising means structure in the selecting specification whether an output signal which performs the is to function of providing an output on be supplied to an output pin а based on contents of terminal, and selecting said output control memory whether or not to

cell:	supply the	
,	output signal to an	
	output signal to an	
	based on the contents	
	of an	
	or all	
	output control memory	
	I ne structure disclosed	
	specification is the	
	entire	
	circuit of Figure 16	
	except	
	the "Input Circuit	
	(Figure	
	9)". 9:57-10:11.	
first switching means	A structure which is	
	the same	
responsive to a control	as or the equivalent of	
sıgnal	the	
coupled to and	structure in the	
responsive to	specification	
contents of said storage	which performs the	
	function of	
selection memory cell,	connecting either a	
said	first data	
first switching means	signal from the sensing	
	means	
operative to couple	or a data signal	
either	temporarily	
said first data signal or a	stored in the signal	
	storage	
data signal temporarily	means to the output	
stored	terminal	
in said first signal	means, and performing	
storage	that	
means to said first	function based on the	
output	contents	
terminal means;	of a storage selection	
	memory	
	cell. The structure	
	disclosed	
	in the specification is	
[	the	
	OMUX of Figure 14.	
	9:9-44.	
--------------------------------	-----------------------------	--
and feedback switching	A structure which is	
means	the same	
responsive to contents	as or the equivalent of	
of said	the	
feedback control	structure in the	
memory cell	specification	
and operative to couple	which performs the	
or not	function of	
couple said first data signal	connecting the data signal	
to said AND array.	from the sensing	
	means to the	
	AND array, and	
	selecting	
	whether or not to	
	connect the	
	data signal based on the	
	contents of a feedback	
	control	
	memory cell. The	
	structure	
	disclosed in the	
	specification	
	is the FMUX of Figure	
	15.	
The '4	21 Patent	
Patent '421 Claim 1	Construction	
In a programmable logic device	This is a "Jepson" claim in	
including a plurality of	that it begins with a	
•	preamble	
electronic logic circuit means	that recites an old device,	
each having data input.	continues with a transition	
output, and input/output	that states "an improved	
terminals, and having	programmable means	
signal	comprising"	
feedback paths to said	and concludes with the	
data	body of	
input terminals, and	the claim as the statement	
being	of	
responsive to input data	the new improvements	
r to to mpat and	upon the	

signals received at said data	old device.
input and input/output	
terminals and operative	The limitations impose
to	the
perform particular logic	preamble include "electronic
functions and to	logic circuit means"
generate	elements

generate commensurate circuit means output signals, and

ed by elements which perform the function of responding to input data signals and operating to perform logic functions and to generate output signals. This claim covers a structure which is the same as or the equivalent of the structure in the specification which performs the function described above. The structure disclosed in the specification is Figure 8A (except elements 80, 82 and 88), or Figure 8B (except the D-F.F. (FIG.13) elements, the OMUX (FIG.14) elements, and the two columns of elements to the far left of the Figure, one labeled "Input Circuit (Fig.9)" and the other labeled "Row Driver (Fig. 10)"), which by reference incorporate Figures 9-12,

 15
 and 16. 3:33-38.
The structures of Figure
8A
and 8B include a
$\Delta ND arrow an OP/NOP$
array a
feedback row driver an
I/O
driver and input circuit,
and
a feedback multiplexer.
7:3-7.
The device must include
more
than one "electronic logic
circuit means" element,
and
each such element must
data input terminals data
output terminals, data
input/output terminals, data
input/output terminals, and
signal feedback paths to
dete input terminals
uata input terminais.
Data input terminals are
Data input terminais are
structures that can be used
w input a signal to the
"alastronia lagia siravit
means" elements.
Data output terminals are
structures that can be used
to
output a signal from the
"electronic logic circuit
means" elements.

	Data input/output terminals
	are structures that can be
	used to input a signal,
	output
	a signal, or both, to or
	from
	the "electronic logic circuit
	means" elements.
	Signal feedback paths are
	circuitry that a signal goes
	through as it passes back to
[	a
	data input terminal.
programmable means for	The "programmable means" of
configuring the	the preamble is a means-
architecture	plus-function
of said logic device so	element.
that	
each said logic circuit	
means	Whitten in Lengen style
is operative to perform a	this
particular logic function,	claim is for an improved
an improved programmable means	programmable means, which
comprising:	performs the function of
	configuring the architecture
	of the device so that each
	"electronic logic circuit
	means" element performs a
	particular logic function.
	The body of the claim
	defines
	the improved
	programmable
	means that performs this
	function.
a plurality of architecture	The programmable means

control circuits each	includes more than one
including:	architecture control circuit
	as further described in the
	claim elements that follow.
a reprogrammable memory device	Each architecture control
having an output terminal and	circuit must have a
having a programming potential	reprogrammable memory device
input terminal by which said	having an output terminal and
memory device may be	a programming potential input
programmed to either a first	terminal.
state to generate a logic	
signal of a first level or programmed to a second state	An output terminal is a structure that can be used to
to generate a logic signal of	output a signal from the
a second level at said memory	reprogrammable memory device.
device output terminal;	
	"Programming potential" is a
	high voltage (for instance 21
	volts in a circuit that
	normally operates at between 0
	and 5 volts) that is required
	to program the memory device.
	4:35-45; 10:36-62.
	A "programming potential input
	terminal" is a terminal
	connecting the
	programming
	potential to the memory

	device.
	The requirement that the reprogrammable memory device
	have a programming potential
	input terminal limits the
	range of covered devices to
	those that require a
	programming potential. SRAM
	memory cells do not require a
	programming potential as that
	term is defined in the
	specification.
programming means responsive	A structure which is the same
to input program data signals	as or the equivalent of the
and to an address signal	structure in the specification
corresponding to said	which performs the function of
reprogrammable memory device	programming the memory device
and operative to	by applying a
program said	programming
memory device by	potential to the
applying a	programming
programming potential to said	potential input terminal. The
memory device programming	structure disclosed in the
potential input terminal;	specification is: transistor
<b>~ *</b> '	N1 whose gate is
	connected to
	line 100 of Figure 24;
	circuitry to raise
	ARDTCNTL of
	Figure 24 to a

	programming
	potential; an "Architectural
	Program Decoder (Fig.20) and
	a [programming potential]
	level shifting circuit similar
	to the Dece Cate Driver
	(Figure 22A)" connected to
	PADFEED of Figure 24;
	and a
	similar
	to that shown in Fig. 21"
	connected to line 14H10 of
	Figure 24 14:26-37
sense means coupled to	A structure which is the
said	same
memory device output	as or the equivalent of the
terminal	1
for sensing the level of a	structure in the
-	specification
logic signal generated by	which performs the
said	function of
programmed memory device and	sensing the level of a logic
for developing a commensurate	signal generated by the
control signal; and	programmed memory device and
	developing a
	commensurate
	control signal. The
	structure
	disclosed in the
	specification
	is the Schmidt trigger
	202 of Figure 24. 14:16-18.
multiplexer means	A structure which is the
responsive	same
to said control signal and	as or the equivalent of the
operative to couple said	structure in the
logic	specification

circuit means output	which performs the	
terminal	function of	
either to an input/output	coupling the logic circuit	
terminal or to a signal	means output terminal either	
feedback path thereby	to an input/output terminal	
causing	or	
said logic circuit means to	to a signal feedback path	
have one of a	thereby causing the logic	
predetermined	• • • • •	
set of logic circuit	circuit means to have one of a	
configurations.	predetermined set of logic	
	configurations. The	
	structure	
	disclosed in the	
	specification	
	is the FMUX of Figure 15.	
	9:63-10:5.	
Patent '421 Claim 7	Construction	
In a programmable	See claim 1.	
logic device		
as recited in claim 1		
wherein said logic	See discussion of	
circuit	"electronic	
means includes	logic circuit means" in claim	
register means for	1 above. The	
temporarily	"electronic	
storing said circuit	logic circuit means"	
means	elements	
output signal and for	must include a	
	structure which	
developing a stored output	is the same as or the	
signal, and	equivalent of the	
signal, and	structure	
	disclosed in the	
	specification	
	which performs the	
	function of	
	temporarily storing the	
	"electronic logic	

	circuit
	means" element output
	signal
	and developing a
	stored output
	signal The structure
	disalaged in the
	disclosed in the
	is the D Elin Elen of
	Eiguro
	$\frac{12}{12} 0.7 16$
1 • • 1	13. 9:7-10.
wherein said	See discussion of
multiplexer means	multiplexer
includes a plurality of	means" in claim 1
······	above. The
transistor switching	multiplexer means of
means	
connected between a	must include more
plurality	than one of
of data signal	the structures which
receiving	are the
terminals and a	same as or the
multiplexer	equivalent of
output terminal, said	the structures in the
data	
signal receiving	specification which
terminals	perform
being coupled to	the function of
receive said	conducting or
circuit means output	not conducting a data
sıgnal,	sıgnal
said stored output	so as to allow the
signal and	multiplexer
an input signal from	means to selectively
said	connect a
input/output terminal,	data signal to the
each	multiplexer
said switching means	output terminal. The
being	
coupled to receive a	particular data signal
control	to be
signal from one of	connected is (1) the
said	circuit
architecture control	means output signal;
circuits	(2) the

whereby one of said	stored output signal;
switching	or (3)
means may be	an input signal from
rendered	an
others of	The
said switching means	selection of which
may be	data signal
rendered	to connect is
nonconductive by	determined by
appropriately	control signals from
programming the	the
corresponding	architecture control
reprogrammable	circuits,
memory device.	which in turn are
	derived from
	the contents of the
	corresponding
	reprogrammable
	memory device. The
	structure
	disclosed in the
	specification
	is the multiplexer of
	Figure
	15. The structures
	in the specification as
	the
	means are
	switching transistors
	such as
	those labeled "N" in
	Figure
	15.
Patent '421 Claim 13	Construction
In an integrated circuit	This is a "Jepson" claim in
device including	that it begins with a
electronic	preamble
logic circuit means	that recites an old device,
having	
data input, output, and	continues with a transition
input/output terminals,	that states "an improved

and	
signal feedback paths to said	programmable means comprising"
data input terminals, and	and concludes with the body of
being responsive to at least	the claim as the statement of
one architecture control	the new improvements upon the
signal and operative to perform a particular	old device.
electronic function on at	The limitations imposed by the
least one input data signal	preamble include an
received at a data input	"electronic logic circuit
terminal to generate at least	means" element which responds
one commensurate circuit means	to at least one architecture
output signal at said circuit	control signal and which
means output terminal, and	performs the function of
	operating to perform a
	particular electronic function
	on at least one input data
	signal to generate at least
	one commensurate circuit means
	output signal. This claim
	covers a structure which is
	the same as or the equivalent
	of the structure in the
	specification which
	performs
	the function described above.
	The structure disclosed in the
	specification is Figure 8A

(except elements 80, 82	
and 88) or Figure 8B (except	
the	
D-F.F. (FIG.13) elements,	
the	
OMUX (FIG.14) elements,	
and	
the two columns of	
elements to	
the far left of the Figure,	
one labeled "Input Circuit	
(Fig.9)" and the other	
labeled "Row Driver (Fig.	
10)"), which by reference	
incorporate Figures 9-12,	
15	
and 16. 3:33-38.	
The structures of Figure	
δA and 8D include a	
and ob include a	
AND array an OR/NOR	
array, a	
feedback row driver, an	
I/O	
driver and input circuit,	
and	
a feedback multiplexer.	
7:3-7.	
The "electronic logic	
circuit	
means" element must have	
data	
input terminals, data output	
terminals, data input/output	
terminals, and signal feedback	
paths to the data input	
terminals	
Community.	

Data input terminals are

	structures that can be used to input a signal to the "electronic logic circuit means" element.
	Data output terminals are structures that can be used
	to
	"alectronic legic circuit
	"electronic logic circuit
	means" element.
	Data input/output terminals
	are structures that can be
	used to input a signal, output
	a signal, or both, to or from
	the "electronic logic circuit
	means" element.
	Signal feedback paths are
	circuitry that a signal goes
	through as it passes back to
1 • 11	data input terminal.
naving programmable	The "programmable means" of
providing said	the preamble is a means
architecture	plus-function
control signal to	element.
configure	
the architecture of said	
logic	
device so that said circuit	Written in Jepson-style, this
means will perform a	claim is for an improved
particular electronic	programmable means, which
function, an improved	performs the function of
programmable means	providing an architecture

comprising:

	control signal to configure
	the architecture of the device
	so that the "electronic logic
	circuit means" element
	performs a particular
	electronic function. The body
	of the claim defines the
	improved programmable means
	that performs that function.
at least one architecture	The "reprogrammable memory
control circuit including:	device," "programming means,"
a reprogrammable	and "sense means"
memory device	elements of
having an output terminal and	this claim have the same
a programming potential input	meaning as the corresponding
terminal and which may be	elements of claim 1.
programmed either to a first	
state to generate a logic	
signal of a first level or	
programmed to a second state	
to general a logic signal of a	
second level at said memory	
device output terminal;	
programming means responsive	
to input program data signals	
and to a corresponding address	
signal and operative to	

program salu memory device to one of said states by applying a programming potential to said memory device programming potential input terminal; and sense means for sensing the level of a logic signal generated at said programmed memory device output terminal and for developing therefrom said architecture control signal for configuring the architecture of said logic device so that said circuit means will perform a particular electronic function. Patent '421 Claim 16 Construction In an integrated See claim 13. circuit device as recited in claim 13 See discussion of wherein said "electronic electronic logic circuit means logic circuit means" in claim includes multiplexer means 13 above. The responsive "electronic to said architecture logic circuit means" element control signals and operative must include a structure which to couple said circuit is the same as or the

means	
output terminal either	equivalent of the
to an	structure in
input/output terminal	the specification
or to a	which is
signal feedback path.	responsive to the
	architecture
	control signals and
	which
	performs the function
	of
	connecting the
	"electronic
	logic circuit means"
	element
	output terminal either
	to an
	input/output terminal
	or to a
	The
	structure disclosed in
	the
	specification is the
	OMUX of
	Figure 14 and the
	FMUX of
	Figure 15.
Patent '421 Claim 19	Construction
In an integrated circuit	See claim 16.
device as recited in claim 16	m
wherein said	See discussion of
programmable	
means includes a	"programmable
plurality of	means" and
architecture control	"architecture control
circuits	
	circuits" in claims 1
	and 13
	above. The
	"programmable
	means" element must
	include
	more than one

	architecture
	control circuit.
and wherein said	The "register means"
electronic	element
logic circuit means	of this claim has the
further	same
includes register means	meaning as the
for	corresponding
temporarily storing said	element of claim 7.
circuit means output	
terminal	
signal and for	
developing a	
stored output signal,	
and wherein said	The "multiplexer
multiplexer	means"
means includes a	element of this claim
plurality of	has the
transistor switching	same meaning as the
means	
connected between a	corresponding element
plurality	of claim
of data receiving	7.
terminals	
and a multiplexer output	
terminal, said data	
receiving	
terminals being coupled	
to	
receive said circuit	
means	
output terminal signal,	
said	
stored output signal and	
an	
input signal from said	
input/output terminal, each	
said transistor switching	
means being coupled to	
means being coupled to	
from	
IIOIII	
one of said architecture	

control circuits whereby	
one	
of said switching means	
may be	
rendered conductive and	
the	
others of said switching	
means	
may be rendered	
nonconductive	
by appropriately	
programming	
the corresponding	
reprogrammable memory	
devices.	
Patent '421 Claim 25	Construction
In an integrated circuit	See claim 16.
device as recited in claim	
16	
wherein said	See discussion of
programmable	
means includes a	"programmable means"
plurality of	in claims
architecture control	1 and 13 above. The
circuits,	
	"programmable means"
	element
	must include more than
	one
	architecture control
	circuit.
and wherein said	The "register means"
electronic	element
logic circuit means	of this claim has the
further	same
includes register means	meaning as the
for	corresponding
temporarily storing said	element of claim 7.
circuit means output	
signal	
and for developing a	
stored	
output signal,	
and wherein said	The "multiplexer
multiplexer	means"

means includes output	element of this claim has the
multiplexer having a plurality	same meaning as the
of transistor switching means connected between a plurality	corresponding element of claim 7.
of data receiving terminals	
and a multiplexer output	
receiving	
terminals being coupled	
to	
receive said circuit	
means	
output signal, said stored	
output signal and an	
input	
signal from said	
terminal each said	
switching	
means being coupled to	
receive	
a control signal from	
one of	
said architecture control	
circuits whereby one of	
said	
switching means may be	
rendered conductive and the	
others of said switching	
means	
may be rendered non-	
conductive	
by appropriately	
programming	
the corresponding	
reprogrammable memory devices	

The '986 Patent		
Patent '986 Claim 1	Construction	
A programmable	A programmable	
integrated	integrated	
circuit logic array	circuit logic array	
device,	device is	
comprising:	an integrated circuit	
	that can be	
	programmed to	
	perform various logic	
	functions	
a plurality of input	An input terminal is a	
terminals	An input terminar is a	
for receiving input	structure that can be	
signals;	used to	
	input a signal. The	
	device	
	must have more than	
	one input	
	terminal.	
a plurality of I/O	An I/O terminal is a	
terminals	structure	
for receiving input	that can be used to	
signals	input a	
and/or transmitting	signal, output a signal,	
output	or	
signals;	both, to or from the	
	device.	
	The device must have	
	more than $I(O_{1}) = \frac{1}{2}$	
C' ( 1 1') C	one I/O terminal.	
first plurality of	A macrocell 1s a	
macrocells	repeating	
each including	block of circuit	
	elements (as	
	described below)	
	which	
	includes the wiring	
	necessary	
	to connect the	
	elements.	
at least a first	The "first	
programmable	programmable AND	
AND array having a	array" element of this	

first	claim
plurality of memory	has the same meaning
cells	as the
arranged in	corresponding element
addressable rows	of
and columns, each said cell	patent B1'479 claim 1. The
being individually	term "each said
	memory cell
programmable to contain logic	being individually
data corresponding to	programmable to
the	contain logic
memory state of the	data" has the same
cell,	meaning as
	the term "which can be
	individually
	programmed to
	contain logic data" in
	patent
	B1'479 claim 1.
first sensing means	A structure which is
connected	the same
to said first AND	as or the equivalent of
array, said	the
first sensing means	structure in the
being	specification
responsive to certain	which is responsive to
ones of	certain
said input signals and	ones of the input signals and
operative to detect the memory	which performs the function of
state of one or more of said	detecting the memory state of
cells and to develop a	one or more of the memory
corresponding first data	cells, and developing a
signal.	corresponding first
0,	data
	since 1. The strategies
	signal. The structure
	disclosed in the

	is standard circuitry to
	implement an OR gate
	and a
	sense amplifier. 5:13-
	IJ; Eig 2 alamant 66 and
	Fig. 2 element 66, and Fig. 3.
first signal storage	A structure which is
means,	the same
	as or the equivalent of
	the
	structure in the
	specification
	which performs the
	function of
	storing a signal. The
	structure disclosed in the
	specification is the D Flip-Flop
	shown as element 76
	of
	Figure 3 5.18
first feedback means	A structure which is
mot recubick mount,	the same
	as or the equivalent of
	the
	structure in the
	specification
	which performs the
	function of
	feeding back signals. The
	structure disclosed in the
	specification is a
	connection
	between the feedback
	multiplexer and a row driver.
	See Figs. 2-5.
and first multiplexing	This means-plus-
means	function claim
for selectively	language requires a

coupling said	structure
first data signal to one of	which is the same as or the
said I/O terminals, to said	equivalent of a structure in
first storage means, or	the specification which
said first feedback	performs the function
incano, and	selectively coupling the first
	data signal developed by the
	sensing means to an I/O
	terminal, to the storage
	means, or to the feedback
	means. There is no
	structure
	in the specification which
	performs this function.
	The Court notes that the
	specification discloses
	a
	structure that performs
	a
	similar, although
	different function The
	text
	and drawings of the
	specification portray a
	structure that
	continuously
	connects the first data
	signal
	to the storage means.
	The
	selectivity provided by

	disclosed multiplexing means allows coupling of: (1) either the first data signal or the output of the storage means to the I/O terminal; and (2) either the output of the
	storage means or the I/O terminal to the
	teedback means. The structure
	disclosed in the specification which performs these functions is the feedback
	multiplexer
	labeled 93 and the
	multiplexer labeled 91 of
	Figure 3. 4:59-62; 5:25-28.
	34-36.
a plurality of data	A data bus is "one or
including	conductors that are used for
	transmission of data " The IEEE Standard
	Dictionary of Electrical and
	<i>Electronics Terms</i> , 117 (6th
	ed.1996).
a global input signal bus for	A global input signal bus is a
coupling input signals	data bus that couples

from	input
said input terminals to	terminals to all AND
a	arrays on
first group of cells in	the device $6.42-44$
the	Fig. 5.
AND arrays of each	8
said	
macrocell	
a local feedback bus	A local feedback bus is
Ior	a data
coupling signals	bus that couples
applied to	feedback
the feedback means of	signals to a subset of
at least	the AND
some of said	arrays on the device.
macrocells to a	6:49-54.
second group of cells	See also 4:25-28;
of at	5:37-42;
least some of said	Figs. 1 and 5.
macrocells.	
and a global feedback	A global feedback bus
bus for	is a
coupling data signals	data hus that couples
applied	feedback
applied	signals from a subset
reedback means	
to a third group of	macrocells to all AND
cells of	arrays
all of said AND arrays	on the device. 6:45-48.
of said	See
macrocells.	also 4:28-34; 6:33-35;
	Figs. 1
	and 5.
Patent '986 Claim 2	Construction
A programmable	See claim 1.
integrated	
circuit logic array device	
as	
recited in claim 1 and	
further	
comprising.	
a sacond plurality of	The "programmable
a second pluranty of	AND array",
macrocells each	"second sensing means",
including a	-

programmable AND	"second signal storage
array having	means",
a plurality of memory	terminal
arranged in addressable	means" and "second
rows	means, and second
and columns, each said	multiplexing means" all
cell	have
being individually	the same meaning as the
programmable to	corresponding elements
contain logic	of
data corresponding to the	claim 1.
memory state of the cell	
second sensing means	The device must include
	a
responsive to certain	second set of macrocells
ones of	as
said input signals and	those are described in
	claim
operative to detect the	1.
memory	
state of one or more of	
salu and to develop a	
corresponding data	
second signal storage	
means.	
seconds feedback	
terminal	
means, and second	
multiplexing	
means for coupling said	
second	
data signal to said	
second	
storage means or to said	
second feedback means.	
Patent '986 Claim 12	Construction
A programmable integrated	See claim 1.
circuit logic array	

device as	
recited in claim 1 and	
further	
comprising:	
a plurality of input	An input latching
latching	circuit is
circuits each coupling	standard circuitry
one of	that
said input terminals to	captures and holds
said	input
input signal bus	signals, 7:22-45:
whereby input	Fig. 6.
signals applied to said	1.8. 01
input	
terminals are	
maintained	
stable during certain	
intervale of time	
Intervals of time.	Construction
Patent 986 Claim 13	Construction
A programmable	See claim 12.
integrated	
circuit logic array	
device as	
recited in claim 12	
wherein said input	The input latching
latching	circuits
circuits include one	must contain one
input	input level
level shifting	shifting inverter
inverter stage,	stage, an
an output driver	output driver
element, and	element, and a
a switchable pass	switchable pass gate
gate and	and latch
latch coupling the	which couples the
inverter	inverter
stage to the driver	stage to the driver
element.	element.
	See, e.g., Fig. 6;
	7:22-45.
Patent '986 Claim 14	Construction
A programmable	See claim 1.
integrated	
circuit logic arrav	
device as	

recited in claim 1	
wherein said first	See discussion of
multiplexing means	"multiplexing means"
includes a	in claim
first switching means	1 above. The
for	"multiplexing
connecting either the	means" element must
output	include a
of said first sensing	structure which is the
means or	same as
the output of said first	or the equivalent of
1	the
signal storage means	structure in the
to one of	specification
said I/O terminals.	which performs the
	function of
	connecting either the
	output
	of the "first sensing
	means"
	element or the output
	of the
	"first signal storage
	means"
	element to one of the
	I/O
	terminals. The
	structure
	disclosed in the
	specification
	is the output
	multiplexer 91
	of Figure 3.
Patent '986 Claim 15	Construction
A programmable	See claim 14.
integrated	
circuit logic array	
device as	
device as recited in claim 14	
device as recited in claim 14 wherein said first	See discussion of
device as recited in claim 14 wherein said first multiplexing means	See discussion of "multiplexing means" in
device as recited in claim 14 wherein said first multiplexing means further	See discussion of "multiplexing means" in claims
device as recited in claim 14 wherein said first multiplexing means further includes a second	See discussion of "multiplexing means" in claims 1 and 14 above. This means-
device as recited in claim 14 wherein said first multiplexing means further includes a second switching	See discussion of "multiplexing means" in claims 1 and 14 above. This means- plus-function

couple	
either the output of said	requires a structure which is
first sensing means or one of	the same as or the equivalent
said I/O terminals to said	of a structure in the
first feedback means.	specification which performs
	the function of coupling the
	output of the sensing means or
	the output of one of the I/O
	terminals to the feedback
	means. There is no structure
	in the specification which
	performs this function.
	The Court notes that the
	specification discloses a
	structure that performs a
	similar, although somewhat
	different, function. The text
	and drawings of the
	specification portray a
	structure that allows coupling
	of either the output of the
	storage means or the output of
	one of the I/O terminals to
	the feedback means. The
	structure disclosed in the
	specification which performs
	this function is the feedback
	multiplexer labeled 93 in
	Figure 3. 4:59-62; 5:25-28,

34-36.

IT IS SO ORDERED.