United States District Court,
E.D. New York.

LORAL FAIRCHILD CORPORATION,
Plaintiff.
v.
VICTOR COMPANY OF JAPAN, LTD., et al,
Defendants.
LORAL FAIRCHILD CORPORATION,
Plaintiff.
v.
MATSUSHITA ELECTRIC INDUSTRIAL COMPANY, LTD., et al,
Defendants.

Civ. A. Nos. 92-0128-ARR, 91-5056-ARR

Oct. 18, 1995.

Patent holder sued various defendants for infringement of two patents. In preparation for trial, the District Court, Rader, Circuit Judge, sitting by designation, interpreted several disputed terms in the patents.

Ordered accordingly.

3,896,485, 3,931,674. Construed.

James H. Wallace, Jr., John B. Wyss and Gregory Lyons of Wiley, Rien & Fielding, Washington, DC; and Anthony W. Karambelas of Newport Beach, California, for plaintiff.

Douglas B. Henderson, Barry W. Graham, Robert E. Converse, Jeffrey A. Berkowitz and Vincent P. Kovalick of Finnegan, Henderson, Farabow, Garrett & Dunner, Washington, DC, for the Sony defendants.

Arthur I. Neustadt of Oblon, Spivak, McClelland, Maier & Neustadt, P.C., Arlington, Virginia, for the Toshiba defendants.

John B. Pegram and Andrew T. D'Amico, Jr. of Fish & Richardson, P.C., New York City, for the Sanyo defendants.

William A. Streff, Jr. of Kirkland & Ellis, Chicago, Illinois, and John Donofrio of Kirkland & Ellis, New York City, for the Hitachi defendants.

Marvin N. Gordon of Hopgood, Califafde, Kalil & Judlowe, New York City, for the NEC defendants.

Jared B. Bobrow, and Matthew D. Powers of Weil, Gotshal & Manges, Menlo Park, California, for the OKI defendants.

RADER**, Circuit Judge (Sitting by Designation).**

In this patent case, Loral Fairchild Corp. (Loral) alleges that numerous defendants have willfully infringed United States Patents 3,931,674 (the '674 patent) and 3,896,485 (the '485 patent). The defendants deny liability and have asserted that the claims of the patents are, among other things, invalid and unenforceable. Defendants have also raised claims of laches and estoppel and challenged Loral's ownership of the patents. This court has scheduled this case for trial beginning on January 8, 1996.

The parties have filed motions for a summary judgment on many of the liability issues, including infringement and validity. On August 19 and 20, 1995, the court held a two-day evidentiary hearing to receive testimony from qualified experts about the meaning of the patent claims. This Opinion constitutes the court's conclusions about the disputed terms in the patents.

BACKGROUND

The Technology

The '674 and '485 patents describe inventions in the field of charge coupled devices (CCDs). A charge coupled device is a significant advance over standard semiconductor devices. Like other semiconductor devices, a CCD stores electronic charges in a spatially defined depletion region (potential well) at the surface of the device. The CCD, however, adds the ability to move these stored charges to adjacent wells. Thus, the CCD enables swift transfer and manipulation of the information stored in the form of electronic charges. In a CCD, voltage applied to the surface of the device both forms the potential well for storing charges and regulates transfer of those charges.

CCDs are particularly valuable in light sensing applications and as shift registers. Consumer electronics products such as cameras, VCRs, facsimile machines, and copiers use CCDs to perform their core functions. In simple terms, the light entering the lens of a camcorder registers as a charge on the surface of a photosensor. The intensity and color of the light determine the amount of charge in the light sensing semiconductor. Once the photosensor receives this charge, however, the CCD technology operates to swiftly transfer this same charge to neighboring wells and then off of the semiconductor surface in the form of a digital record. A CCD transports information or charges across the surface of a "chip." This transfer occurs in response to fields applied to the surface of the devices. A CCD uses topographical variations in the semiconductor surface-also known as metal-oxide-silicon (MOS) technology-to control movement of these charge packets.

The Patents

Loral alleges infringement of claim 1 of the '674 patent. On January 13, 1976, the United States Patent and Trademark Office (PTO) issued the '674 patent to Gilbert F. Amelio from an application filed on February 8, 1974. The patent bears the title "Self Aligned CCD Element Including Two Levels of Electrodes and Method of Manufacture Therefor." Amelio assigned his rights to the '674 patent to Fairchild Camera and Instrument Corporation (Fairchild). Loral asserts its ownership in this patent through a series of transfers originating from Fairchild.

The '674 patent claims a process for making a CCD. It contains 9 claims. Claim 1 reads:

1. A process for fabricating a charge coupled device structure in a semiconductor substrate, comprising the steps of

selectively applying at least one layer of insulation material to said semiconductor substrate;

selectively forming a plurality of spaced-apart first gate electrodes on the uppermost surface of said at least one layer of insulation material;

forming a first insulation layer over said plurality of first gate electrodes;

forming implanted barrier regions in said semiconductor substrate in the intervals between said plurality of spaced-apart first gate electrodes, the edges of said implanted barrier regions being aligned with the vertical edges of the insulation layer on the respective first gate electrodes;

selectively forming a plurality of second gate electrodes on said uppermost surface of said at least one insulating layer between said plurality of spaced-apart first gate electrodes, each of said second gate electrodes substantially occupying the space between adjacent first gate electrode; and

connecting each of said second gate electrodes to and individual adjacent first gate electrode to form a composite electrode for a charge coupled element.

In addition, Loral alleges infringement of claims 1, 3, 7, and 8 of the '485 patent. The PTO issued the '485 patent to James M. Early on July 22, 1975, from an application filed on December 3, 1973. The patent bears the title "Charge-Coupled Device with Overflow Protection." Like Amelio, Early assigned his rights in the patent to Fairchild. Similar to the '674 patent, Loral alleges a chain of transfers as its basis for ownership of this patent.

The '485 patent claims an anti-blooming element in a CCD and a method of operating that device. It contains 8 claims. Claim 1 reads:

1. Structure which comprises:

a. a light sensing element comprising a first region of semiconductor material overlaid by a first electrode separated from said semiconductor material by insulation, said light sensing element being capable of containing a charge packet;

b. an adjacent region of said semiconductor material disposed for receiving said charge packet from said light sensing element;

c. means for controlling the transfer of said charge packet from said light sensing element to said adjacent regions; and,

d. charge sink means having a contact for applying a bias thereto buried within said semi-conductor material and disposed for receiving excess charge accumulated in said light sensing element, said charge sink means extending laterally from said contact toward said light sensing element while beneath the surface of said

semiconductor material.

Claim 3, which depends from claim 1 reads:

3. Structure as defined in claim 1, wherein said charge sink means comprises a region of conductivity type opposite to that of said semiconductor material.

Claim 7, another independent claim in the '485 patent reads:

7. A method of operating a charge-coupled imaging device formed in semiconductor material containing at least one light sensing element and a charge sink region having a contact for applying a first potential thereto located beneath the surface of said semiconductor material and extending laterally from said contact toward said at least one light sensing element, which comprises:

a. accumulating packets of charge in said at least one light sensing element; and,

b. allowing excess charges within said at least one light sensing element to transfer to said charge sink region by applying said first potential to said charge sink region during a selected time interval.

Claim 8, which depends from claim 7, reads:

8. A method as defined in claim 7 further including the step of preventing the accumulation of said packets of charge within said light sensing element by applying a second potential to said charge sink means during a second time interval.

The Markman Trial

During pendency of this action, the Court of Appeals for the Federal Circuit decided Markman v. Westview Instruments, Inc., 52 F.3d 967 (Fed.Cir.1995), *petition for cert. granted,* 515 U.S. 1192, 116 S.Ct. 40, 132 L.Ed.2d 921 (1995). The Federal Circuit in *Markman* clarified that, in a case tried to a jury, a trial judge must now interpret the meaning of words in a patent claim as a matter of law and instruct the jury accordingly: "[I]nterpretation and construction of patent claims, which define the scope of the patentee's rights under the patent, is a matter of law exclusively for the court." *Id.* at 970-71. In accordance with *Markman,* this court examined extensive briefing on pending summary judgment motions and requested additional briefing on the meaning of the claims.

The extensive briefing convinced this court of the need for expert testimony to enlighten the meaning of claim terms to one of ordinary skill in the art at the time of invention. As a result, the court held a two-day bench trial on September 19 and 20, 1995. The court permitted each side to present two expert witnesses. These experts were extensively examined and cross-examined.

Loral called Dr. David Wen to testify on the '674 patent and Dr. David F. Barbe to testify on the '485 patent. Defendants, collectively, called Dr. James N. Fordemwalt to testify on the '674 patent and Dr. Robert W. Bower to testify on the '485 patent.

Dr. Wen holds a bachelor of science degree, a master of science degree, and a doctorate in philosophy in electrical engineering from the University of California at Berkley. He currently is the Director of

Engineering for Loral Fairchild Imaging Sensors, part of Loral. Dr. Wen has worked for more than twenty-one years in the area of charge coupled device technology.

Dr. Barbe, Loral's other witness, holds a bachelor of science degree and a master of science degree in electrical engineering from West Virginia University. He also holds a doctorate in philosophy in electrical engineering from The Johns Hopkins University. Dr. Barbe is the executive director of the engineering research center at the University of Maryland.

Defendants' witness, Dr. Fordemwalt, holds a bachelor of science degree in chemistry and a master of science degree in analytical chemistry from the University of Arizona. He also holds a doctorate in philosophy in physical chemistry from the University of Iowa. Dr. Fordemwalt has worked for more than twenty years in the field of semiconductor fabrication processes. He is associate program coordinator for microelectronics and coordinator of graduate studies at the Arizona State University.

Finally, Dr. Bower, also a defendants' witness, holds a bachelor of arts degree in physics from the University of California at Berkley. He also holds a master of science degree in electrical engineering and a doctorate in philosophy in applied physics from the California Institute of Technology. Dr. Bower is a professor in the electrical and computer engineering department of the University of California at Davis.

DISCUSSION

The parties interpret differently the meaning of four portions of each patent. The court will first address the legal requirements of claim construction. It will then address each significant dispute over the meaning of claim terms in turn.

Claim Construction

[1] Claim interpretation elaborates on an inventor's "normally terse language" in the patent claims, in order to understand and explain, but not to change, the scope of those claims. Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1580 (Fed.Cir.1991). A number of factors may help construe or interpret claim terms, including other words in the claim, other claims in the patent, the specification, the prosecution history, and expert testimony and other evidence outside the patent. SmithKline Diagnostics, Inc. v. Helena Labs. Corp., 859 F.2d 878, 882 (Fed.Cir.1988).

[2] [3] As an independent lexicographer in authoring a patent, an inventor may freely define claim words. However, the specification or prosecution history must clearly explain any special definitions or usages in a claim. Markman, 52 F.3d at 980; Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388 (Fed.Cir.1992). In other words, where the inventor does not clearly explain the adoption of an uncommon or new definition for a claim term, the common meaning of that term to one of ordinary skill in the art controls. Beachcombers v. WildeWood Creative Prods., Inc., 31 F.3d 1154, 1158 (Fed.Cir.1994).

[4] [5] While other claims may supply insight into the scope of a claim, Fromson v. Advance Offset Plate, Inc., 720 F.2d 1565, 1570 (Fed.Cir.1983), this court may not read narrow claim limitations into broad claims during either a validity or an infringement analysis. SRI Int'l v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1122 (Fed.Cir.1985). Examples set forth in the specification do not necessarily limit the scope of a claim. Transmatic, Inc. v. Gulton Indus., Inc., 53 F.3d 1270, 1277 (Fed.Cir.1995).

[6] [7] A patent's prosecution history also influences the interpretation of claim language. Markman, 52 F.3d

at 980; *accord* Graham v. John Deere Co., 383 U.S. 1, 33, 86 S.Ct. 684, 701, 15 L.Ed.2d 545 (1966); *see* Singer Mfg. Co. v. Cramer, 192 U.S. 265, 278-85, 24 S.Ct. 291, 296-99, 48 L.Ed. 437 (1904). "Although the prosecution history can and should be used to understand the language used in the claims, it too cannot 'enlarge, diminish, or vary' the limitations in the claims." Markman, 52 F.3d at 980. Prosecution history generally operates to foreclose an interpretation disclaimed or disavowed during the process of acquiring a patent. Jonsson v. Stanley Works, 903 F.2d 812, 817 (Fed.Cir.1990). Claim interpretation in view of the prosecution history is a preliminary step in determining literal infringement, while prosecution history estoppel limits application of the doctrine of equivalents after proper interpretation of the claims yields no finding of literal infringement. *See* Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 870 (Fed.Cir.1985).

[8] Extrinsic evidence may demonstrate the state of the art at the time of the invention and thus assist the court in the construction of the patent claims. Markman, 52 F.3d at 980; Brown v. Piper, 91 U.S. 37, 41, 23 L.Ed. 200 (1875). The extrinsic evidence provides assistance to the court in understanding how someone skilled in the art at the time of the invention would understand the claims. Markman, 52 F.3d at 980-81.

The '674 Patent

A. How is Insulation Selectively Applied?

[9] The parties interpret differently whether claim 1 of the '674 patent requires application of insulation only in certain places and not in other locations over the semiconductor substrate. Claim 1 reads, in relevant part, "selectively applying at least one layer of insulation material to said semiconductor substrate." The claim language does not specify locations or methods for application of insulation.

The term "insulation material" has its common meaning: material that does not conduct electricity. The term "selectively applying" has no common, well-understood meaning. Thus, this court sought expert testimony about its meaning to one of skill in this art at the time of invention.

Dr. Wen testified that one skilled in the art at the time of the invention would have understood this process step to encompass formation of one or more layers of a defined thickness of insulation at different points across the surface of the device. Transcript of September 19, 1995, hearing, at 224 (hereinafter referred to as "Transcript"). According to Dr. Wen, the thickness of insulation varies in different parts of the device. For example, the active part of the circuit, where the light sensing element resides, would have a relatively thin layer of insulation material. A thin layer at this location is necessary to facilitate sensitivity to light. However, Dr. Wen explained, the periphery of the device or field area would have a relatively thick layer of insulation. Transcript at 224-25.

Dr. Wen explained that at the time of the '674 patent those in the field knew several methods of applying different thicknesses of insulation at various locations on the device. For example, one application process would grow a relatively thick layer of insulation over the whole array. The manufacturer would then use a mask to define the active region of the circuit. After masking, a chemical etch would remove the thick oxide in these areas. Then, the manufacturer would grow a very thin layer of oxide in the active region. Thus, "selectively applying" as understood by those skilled in the art at the time of invention meant application of a thin layer of insulation over the active region leaving a relatively thick layer in the inactive region. Transcript at 225-26.

The specification also suggests the application of insulation material of various thicknesses according to the function of the underlying semiconductor layers. For instance, the specification discusses use of silicon

nitride to prevent the formation of additional oxide on the insulation layers:

The second insulating layer 26 is silicon nitride because thermally grown oxides will not form on the nitride. Thus the silicon nitride is very useful in protecting the underlying layer 24 from becoming significantly thicker as would normally occur during the subsequent oxidation steps in the process of this invention.

The '674 patent, column 4, lines 31-37.

The specification further discusses the use of silicon nitride to slow oxide growth: "Moreover, since oxides grow much more slowly on a silicon nitride surface, no substantial oxide grows on the top surface of silicon nitride layer 26." Column 5, lines 16-18. As these passages indicate, insulation material grows in all areas even using the disclosed illustrative method. Thus, the specification does not suggest that the inventor intended to limit this process step to one technique or to a process that insulated certain areas and not others.

Consequently, this court concludes this language describes a process step during which one or more layers of insulation material of a defined thickness form at specific locations on the top surface of the silicon wafer.

B. Is Insulation Required Before Implantation?

[10] The parties also dispute whether claim 1 of the '674 patent dictates a process sequence requiring formation of the insulation layer over the first gate electrodes before implantation of the barrier regions. The claim language states, in relevant part:

forming a first insulation layer over said plurality of first gate electrodes; forming implanted barrier regions in said semiconductor substrate in the intervals between said plurality of spaced-apart first gate electrodes, the edges of said implanted barrier regions being aligned with the vertical edges of the insulation layer on the respective first gate electrodes.

As the preamble indicates, claim 1 describes a process for making a charge coupled device (CCD). Predominant language norms suggest recounting process steps in a chronological sequence. A process description flows most naturally from one step in the sequence to the next in chronological order. The process step described third in sequence thus generally precedes the step described fourth. Consequently, common descriptive techniques suggest formation of the insulation layer before implantation of the barrier regions.

Beyond chronological description, however, the language of the claim conveys persuasively the same orderly sequence. In part, it requires, "the edges of said implanted barrier regions *being aligned* with the vertical edges of the insulation layer." (emphasis added). In order to align the edges of the barrier region with the edges of the insulation, the insulation must be in place to provide an edge for alignment. In other words, implantation of the barrier region must follow that with which it must align. Thus, the "being aligned" language of the claim dictates a sequence with application of the insulation layer preceding implantation of the barrier regions.

The specification also supports this reading of the claims. At column 5, lines 4-15, the specification describes formation of the thin oxide layer 53-the first insulation layer of claim 1. Immediately thereafter, at

lines 18-30, the specification recites: "Thereafter, the *next* process step is to implant the desired impurity ions ... so as to form ion-implanted barrier regions 44 ... [which] are vertically *aligned with the respective outer edges* of the thermally-grown thin oxide layer 53." (emphasis added). The specification thus stresses the process sequence with step [3], formation of the insulation layer, followed by step [4], implantation of the aligned barrier regions.

The specification also recites, at column 7, lines 4-6, "the implanted barrier regions 44, 46, 48, and 50 are aligned with the sides of the oxide layer 53." Nowhere does the specification suggest implanting barrier regions before the oxide layer. While recognizing that the specification does not necessarily limit the claims, these specification references inform the claim's meaning.

The '674 patent bears the title "Self Aligned CCD Element...." The term "self aligned" refers to semiconductor processing which deposits material on the structure according to a pattern or stencil, a "mask" in the terms of the art. The specification sets forth one embodiment of the claimed invention at column 4, line 8 through column 7, line 15 and in figures 1-9. Figure 4 illustrates the barrier implantation step of this embodiment. The figure shows ion radiation bombarding the semiconductor to form the barrier region. As shown in Figure 4, the insulation on the gate electrodes-already in place-serves as a mask. As the ion radiates down on the device to form the barrier regions, these regions align themselves with the edges of this insulation material. Figure 4 illustrates that prior formation of the insulation serves to provide self alignment of the barrier regions. Thus, the order of this process-insulation preceding barrier regions-facilitates the patent's key self-aligning feature.

The prosecution history also strongly supports this interpretation. Initially Loral sought allowance of a dependent claim which included the narrow step of "forming a first insulation layer over said first gate electrodes *prior* to the step of forming barrier regions." (emphasis added). On May 14, 1975, the inventor amended this claim. The resulting claim recited, in part, " *forming a first insulation layer over said plurality of first gate electrodes;* forming implanted barrier regions in said semiconductor substrate ... said implanted barrier regions being aligned with the *vertical edges of the insulation layer on the* respective first gate electrodes." (emphasis added). The remarks section states that the addition of the new step "results in the correct recitation that the implanted barriers are aligned with the vertical edges of the first insulation layer over the respective first gate electrode." The remarks also state that the "present invention is directed to a *process sequence* which includes this masking feature." (emphasis added). Thus, the inventor expressly acknowledged both that its claims dictate a process sequence and that the insulation serves as a mask to align the barrier regions.

In folding his narrow claim into a broader claim, the inventor dropped language describing insulation formation as "prior to" barrier regions implantation. Nonetheless the explanation for this amendment in the inventor's remarks to the examiner show that this deletion did not change the meaning of the claim. Instead the inventor noted that the claim explained the sequence so well that the "prior to" reference became unnecessary. The "prior to" reference was unnecessary because the claim clearly described the use of an insulated gate as a mask. That is, the process claim required insulation before implantation. The prosecution history thus supports this court's reading of the sequence requirement of claim 1.

In sum, this court concludes claim 1 describes a process that implants a barrier region in the semiconductor substrate using an insulated gate as a mask. In other words, the insulation material must be in place before implantation of the barrier region.

C. What Constitutes the Uppermost Surface of the Insulation Layer?

[11] The parties dispute whether formation of the first and second gate electrodes must occur on exactly the same surface. The claim recites, in relevant part:

selectively forming a plurality of spaced-apart first gate electrodes on the uppermost surface of said at least one layer of insulation material;

. . . . .

selectively forming a plurality of second gate electrodes on said uppermost surface of said at least one insulating layer between said plurality of spaced-apart first gate electrodes, each of said second gate electrodes substantially occupying the space between adjacent first gate electrode;

According to the claim, the process forms the second gate electrodes on "said uppermost surface of said at least one insulating layer between said plurality of spaced-apart first gate electrodes."

The language "said uppermost surface of said at least one insulating layer" refers to the same place where the process previously formed the first gate electrodes. This language specifies the positioning of the second gate electrodes, but does not limit or specify the number of steps involved in formation of these electrodes. Dr. Wen testified that one skilled in the art would understand that the '674 process envisions many steps not specified in the claim 1 procedure. Dr. Fordemwalt agreed, as well, that the '674 process envisions many intermediate steps. Transcript at 344-45. Counsel for Loral questioned Dr. Fordemwalt, "You could have steps that would add a few additional layers [of insulation]." Dr. Fordemwalt responded that "we are talking a lot of layers." Id. In fact, Dr. Fordemwalt agreed that these intermediate steps may involve cleaning or regrowing portions of the exposed surface of the insulation layer. Id. The nature of the '674 process teaches one skilled in the art that "the uppermost surface of said at least one layer of insulation material" would not and could not be the identical atomic surface originally formed. As Dr. Wen explained, "in a semiconductor process environment, it is basically extremely difficult, if not impossible, to preserve the real atoms on a layer-by-layer basis on the surface of a layer ... it is virtually impossible to have the same exact atoms on the surface." Transcript at 242.

With this understanding of the process from the vantage of a skilled artisan, the claim describes the position for formation of the second gate electrodes between the first gate electrodes. The claim requires this formation on the same material at roughly the same thickness as the material under the first gate electrodes. Transcript at 242-43. One skilled in the art would not understand this language to describe the formation of the second gate electrodes on the exact atomic surface of insulation material on which the first gate electrodes were formed. Nothing in the specification or prosecution history suggests limiting this positioning description to an exact atomic layer formed earlier in the multi-stepped process. Consequently, the court concludes "said uppermost surface of said at least one insulating layer" requires formation of the second gate electrodes betweenthe first gate electrodes on the upper surface of the same continuous insulation layer upon which the first gate electrodes were formed.

D. What is a Composite Gate Electrode?

[12] Finally, the parties interpret differently the location and method for connecting the first and second gate electrodes. Claim 1 requires, in relevant part:

connecting each of said second gate electrodes to an individual adjacent first gate electrode to form a composite electrode for a charge coupled element.

This claim language does not restrict the manner or location of the connection. The connection, however, must form a composite gate electrode.

Figures 9, 11, and 13 in the specification depict connection of adjacent first and second gate electrodes. The specification describes forming a conducting layer over exposed portions of the first and second gate electrodes to electrically connect them. In other embodiments, the specification describes etching off portions of the second insulation layer to create an electrical connection. These illustrative examples depict connection of the first and second gate electrodes over the active region of the device, either by forming the second gate electrodes on exposed portions of the first gate electrodes or by forming a conductive layer over exposed portions of both gate electrodes. The specification does not limit the manner or location of the connection.

During prosecution of the '674 patent, in an amendment, dated May 14, 1975, Loral distinguished its connection of electrodes from United States Patent 3,735,156 ("the Krambeck reference"). The figures in the Krambeck reference show every first gate electrode connected to one bus line and every second gate electrode connected to another bus line. Consequently, Krambeck did not connect adjacent gate electrodes. In other words, Krambeck clocked adjacent gates differently.

In the remarks section of the amendment, the inventor argued: "In the present invention, an individual first gate electrode is connected to an adjacent second gate electrode to form a composite gate electrode.... The composite gate electrodes may be connected together in any desired pattern, e.g., in a one-phase, two-phase or three-phase clocking arrangement." The inventor distinguishes the invention because it "includes the unique and distinctive steps of connecting a single first gate electrode to a single adjacent second gate electrode to form a composite electrode." This remark shows that the inventor considered a composite gate electrode to be adjacent gate electrodes clocked together and nothing more. The inventor made no statement to the examiner about the method or location of the connection. In sum, the prosecution history does not limit the claim to a particular manner or location of connection.

Dr. Wen testified about the understanding of one skill in the art relative to connecting adjacent gates. He persuasively recounted that the Krambeck reference does not connect adjacent first and second gate electrodes to form a composite gate electrode. He also noted that, at the time of the '674 patent, those skilled in the art knew several ways to connect electrodes together. This testimony underscores the absence of any limit in the claims on the way to make connections. Transcript at 244-48.

Consequently, the court concludes this limitation describes a process step which connects each second gate electrode to one, but not both, adjacent first gate electrodes.

The '485 Patent

The parties essentially interpret differently only the last portion of claim 1 of the '485 patent. The last portion of claim 1 reads:

d. charge sink means having a contact for applying a bias thereto buried within said semi-conductor material and disposed for receiving excess charge accumulated in said light sensing element, said charge sink means

extending laterally from said contact toward said light sensing element while beneath the surface of said semiconductor material.

A. Is "charge sink means" a means plus function clause?

[13] The inquiry into the meaning of this claim language begins with examination of whether "charge sink means" describes a means for performing a function under 35 U.S.C. s. 112, para. 6 (1988). Under section 112, an inventor may use functional language to describe an invention. However, title 35 limits the scope of a means-plus-function claim to the "corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. s. 112. The different statutory rule for construing means-plus-function claims requires this court to determine whether this claim which recites some structure falls within the ambit of section 112.

The Federal Circuit has clarified that the recitation of some structure does not remove a claim from the ambit of section 112. Laitram Corp. v. Rexnord, Inc., 939 F.2d 1533, 1536 (Fed.Cir.1991). This court, however, must still confront the question of how much recitation of structure removes a claim from the interpretive requirements of section 112, paragraph 6.

Several other courts have confronted this issue. In Fairchild Semiconductor Corp. v. Nintendo Co., 1994 WL 560607 30 U.S.P.Q.2d (BNA) 1657 (N.D.Cal.), *aff'd,* 39 F.3d 1197 (Fed.Cir.1994) (table), another district court interpreted the language "chute means including a locking means having a detent for engaging said locking recess of said cartridge means to hold said cartridge means in a received position" to include a means-plus-function term. The court first noted that the application used the word "means." Id. at 1660, 1994 WL 560607. The court then noted that the word "locking" was unintelligible without reference to a function. While accepting that the claim contained structure such as "a detent," the court nonetheless applied section 112 to the term "locking means." *Id.*

In AMP, Inc. v. Fujitsu Microelectronics, Inc., 853 F.Supp. 808 (M.D.Pa.1994), still another district court interpreted "bus solder tail means" to fall outside a means-plus-function format. The court found the words "bus solder tail" described a specific structure rather than a function. Id. at 820.

This court's analysis of the application of s. 112 begins with examination of the '485 patent's claim language. The claim expressly uses the term "charge sink means." The word "means" is a significant term of art. The Federal Circuit's decision in *Laitram* suggests that the use of the word "means" presumptively places one within section 112. 939 F.2d at 1536. Inventors are not likely to use such an important legal term unless they intend to place themselves within the ambit of section 112.

The additional language in element d of claim 1 does not set forth a discernible structure. Instead, this additional language describes the location of the charge sink means, not its structure. For example, element d indicates that the "charge sink means" is "buried within" the semiconductor material and "disposed for receiving excess charge." These additional words identify the location of the charge sink means. They do not provide sufficient structure to overcome the presumption that the inventor intended to invoke the rules of s. 112 by using the term "means."

Significantly, even Loral's expert witness described a "charge sink means" as a way of performing a function. The court asked Dr. Barbe to define "charge sink means." Dr. Barbe responded: "It is a way for removing excess charge from the light sensing element which is collecting the charge." Transcript at 211.

Loral's own expert and one skilled in the art understood "charge sink means" to describe a function rather than a structure. Transcript at 211-12. In sum, this court determines that the term "charge sink means" falls within the rules of the sixth paragraph of section 112.

[14] [15] [16] Having determined "charge sink means" describes a means-plus-function element, the court turns to interpreting those words with reference to the structure described in the specification. Valmont Indus., Inc. v. Reinke Mfg. Co., 983 F.2d 1039, 1042 (Fed.Cir.1993). The structure, material or acts described in the specification and equivalents thereof set the bounds of this means-plus-function claim. *Id.* FN1

FN1. However, the final inquiry as to whether an accused element is "an equivalent thereof" is a question of fact. D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1575 (Fed.Cir.1985).

The specification of the '485 patent describes and depicts only one charge sink means. Figure 1 shows a region of highly doped semiconductor material, 14, surrounded by a depletion region, 27, created upon application of a bias to the highly doped region of semiconductor material. The specification further describes the charge sink means as a region formed on the surface of a layer of semiconductor material with an epitaxial layer of semiconductor material formed over the top of the charge sink means and first substrate layer.

The specification describes formation of the charge sink region. The first step implants or diffuses an N type impurity into the first layer of P type semiconductor material to form a high conductivity N+ type region. Next, additional P type semiconductor material is formed over the first layer to cover the charge sink region. The specification then notes that application of a potential forms a depletion region around the charge sink region.

Loral's expert, Dr. Barbe, as noted earlier, viewed the charge sink means in functional terms. When the court asked Dr. Barbe to describe the structure associated with that function, he testified: "The structure, the basic structure is a-one embodiment of the structure, which is shown in figure one of the ['674] patent, is a P/N junction, which is created beneath the light sensing element." Transcript at 211-12. In similar terms, he described the charge sink means as the highly doped region, numbered 14 in Figure 1 of the '485 patent, and its associated depletion region. Transcript at 68.

Dr. Barbe agreed that differences in the type of impurities in the semiconductor substrate occur only at the PN junction between region 14 and regions 11 and 12. Dr. Barbe proceeded to testify in argumentative fashion obviously geared to the outcome of litigation. In this vein, he tried to encompass the depletion region within the structure of the charge sink means. He argued that a bias applied to the charge sink region forces electrons out of the surrounding area to form the depletion region. According to Dr. Barbe, this area constitutes structure and is part of the charge sink means. To the contrary, a depletion region exists at any P/N junction regardless of the application of a bias. In the claimed invention, the depletion region functions to receive excess charges flowing out of the light sensing element. Transcript at 105. As conceded by Dr. Barbe, the depletion region is a region influenced by the application of bias, not a region characterized by a different structure. The depletion region is a functional region, not a structural region.

Dr. Bower convincingly underscored this precise point. On several occasions, he stressed that the depletion region is not structure. During direct examination, he specifically stated that the depletion region is not

structure. Transcript at 136-37. Dr. Bower explained that the doping of the semiconductor material defines atomic structure. This doping makes the semiconductor material N or P type. Transcript at 137. The free electrons do not obey the boundaries defined by the P and N type materials. Instead they "spill over" the boundary between P and N type material. Id.

During cross-examination, Dr. Bower emphasized that "[s]tructures are three-dimensional entities that have geometrical definition that are put into the semiconductor, or built on the semiconductor, and it is applying voltages to those that allow us to cause free carriers to move and congregate in certain areas, or disburse." Transcript at 177. In understanding the structure to be built, one skilled in the art would look to those things that form three-dimensional structures, formed through the use of masks, and processes using those masks. Id. These structures, when given a bias, then function to create depletion regions. Id. The depletion region is an area defined by the function of the structures. In these areas, the structures exert control over free carriers.

Thus, this court concludes that the specification describes the structure of the charge sink means as a region of semiconductor material doped opposite from its surrounding semiconductor material. The charge sink means does not include its associated depletion region.

[17] Claim 3 specifically describes a charge sink means as a region of opposite conductivity to its surrounding semiconductor material. This specific description of the charge sink means in claim 3 does not suggest that the charge sink means in claim 1 is broader than that of claim 3. In this patent, claim 3 does not describe an invention distinct from claim 1. In other words, the doctrine of claim differentiation does not operate to distinguish the more specific language in claim 3 from the language of claim 1. As the Federal Circuit has noted, the doctrine of claim differentiation cannot override the limitations resulting from application of the rules for interpreting means-plus-function limitations. Laitram, 939 F.2d at 1538. In the '485 patent, claim 3 buttresses this court's reading of claim 1 by describing more specifically the structure of the "charge sink means" as disclosed by the structure in the specification.

B. Where is the "charge sink means" located?

[18] Claim 1 describes a charge sink means "buried within said semi-conductor material." It also states that the charge sink means must extend laterally from the contact toward the light sensing element "while beneath the surface of said semiconductor material." The parties interpret the term "buried within" differently.

Before addressing the meaning of "buried within," this court must first determine the meaning of "said semiconductor material." "Said" refers to element a of claim 1. Element a specifies a light sensing element comprising "a first region of semiconductor material overlaid by a first electrode...." The expert witnesses testified that this first region would extend only a few microns below the top surface of the element. The term "said semiconductor material," however, is not limited to a few microns near the surface of the semiconductor substrate. FN2

FN2. Loral did not suggest limiting "said semiconductor material" to a top portion of the substrate such as that depicted by 12 on Figure 1 until this court began to ask questions which suggested that interpretation. When this court recalled Dr. Wen to inquire further about this interpretation, Dr. Wen accepted this interpretation with great reticence and equivocation. After all, the number 12 on Figure 1 is nowhere identified as the region near the surface of the semiconductor material sensitive to light. Moreover, the

number 12 region would be much thicker than the "first region of semiconductor material" in the claim language. Dr. Wen helped show that "said semiconductor material" was not limited to a small portion of the top of the substrate.

The specification shows that the semiconductor material referred to in element d comprises the entire substrate. Column 3, lines 17, read:

The N type impurity forming region 14 will diffuse into layer 12 during and following the deposit of layer 12 over substrate 11. Therefore, region 14 is located near the surface between substrate 11 and layer 12, and not necessarily located solely within substrate 11; *that is, region 14 [the charge sink region] is buried within the semiconductor material.*

(emphasis added). While describing only one embodiment of the invention, this passage clarifies that "buried within" uses the entire substrate as its reference and not simply a top layer. "Said semiconductor material," as clarified by the specification, refers to the "semiconductor material" serving as the substrate for the light sensing element and the rest of the invention. Consequently, the words "said semiconductor material" define the entire semiconductor substrate below the top surface of the device.

With that understanding of semiconductor material, the claim language clearly defines a charge sink means completely surrounded by semiconductor material. The claim describes a charge sink means "buried," "within," and "beneath the surface of said semiconductor material." Standing alone, the single term "buried" or the single term "within" might describe something only partially submerged and still in contact with the surface of the substrate. The use of "within" in conjunction with "buried," however, leaves no question that this claim describes a structure completely surrounded by semiconductor material. The addition of "beneath the surface" further clarifies that the charge sink means is completely submerged and does not contact any surface of the device.

The specification further underscores the meaning of the words of the claim. The passage in column 3, quoted above, describes the charge sink means, 14, as sandwiched between two layers of semiconductor material, 11 and 12 in the Figure. Thus, "buried within" means what it says: semiconductor material completely surrounds the charge sink means. In other words, the significance of "buried within" together with "beneath the surface" requires a charge sink means surrounded by and submerged within the semiconductor material. Indeed, figure 1 of the '485 patent depicts the charge sink means in precisely this location.

The prosecution history also supports this meaning. The original claim read: "charge sink means buried within said semiconductor material and disposed in proximity to said light sensing element for receiving excess charge accumulated in said light sensing element." The examiner rejected this claim as obvious over references showing charge drains in contact with the surface of the semiconductor material. Evidently the examiner overlooked the full significance of the terms "buried within" by noting that the claims did not recite the location of the charge region "other [than] that it be 'within the semiconductor material.' " The examiner anticipated, however, the problem of identifying the location of the charge sink means.

In response to the examiner's concern, the applicant amended the claim to read: "charge sink means buried within said semiconductor material and disposed for receiving excess charge accumulated in said light sensing element, said charge sink means being located beneath and not in contact with the surface of said

semiconductor material." The examiner made no further rejections on this point. In other words, the inventor amended the claim to add "beneath and not in contact with the surface" to clarify the location of the charge sink means.

The examiner's remarks in the initial rejection suggest he did not focus on the term "buried." Instead, the examiner read original claim 1 to cover surface drains. To address this rejection, the inventor narrowed and clarified the meaning of the claim. The inventor's use of the words "buried within" together with "beneath the surface" show an intent to depict the charge sink region, as shown in Figure 1, surrounded completely by semiconductor material and not in contact with any surface of the device.

Finally, the testimony of Dr. Bower instructs further on this point. He explained that one skilled in the art would read the words "buried within" to describe a structure completely surrounded by material. In fact, while recognizing "buried within" is not a term of art, an artisan in 1973 would read those words and think of a "buried layer." A buried layer, Dr. Bower explained, is a structure associated with bipolar technology that is completely surrounded by material. Transcript at 138-40.

C. What is "a contact"?

[19] [20] The parties also read "a contact" differently. Element d of claim 1 describes a charge sink means "having a contact for applying a bias thereto." The indefinite article "a" when used in a claim normally means one or more. North Am. Vaccine, Inc. v. American Cyanamid Co., 7 F.3d 1571, 1576 (Fed.Cir.1993), *cert. denied,* 511 U.S. 1069, 114 S.Ct. 1645, 128 L.Ed.2d 365 (1994).

The specification describes the contact shown in Figure 1. It reads, at column 3, lines 24-27:

In accordance with one embodiment, N+ type material, such as phosphorous, is implanted or diffused into layer 12 for forming region 16 which makes ohmic contact with region 14.

It then reads, at lines 27-30: "Other electrical connecting means may be employed for making ohmic contact with region 14. This structure provides a means for externally applying an electrical potential to region 14...." The discussion in the specification describes generally the single illustrative embodiment depicted in the patent. At the same time, the specification states that skilled artisans will know to employ "other electrical contacting means" to supply a bias to the charge sink means. Nothing in the specification limits the claim to a single contact or to a particular kind of contact. Neitherthe applicant nor the examiner focused on "contact" during the course of the prosecution.

The specification suggests that skilled artisans would know many ways to make electrical contact. Dr. Barbe agreed that one skilled in the art would understand that contacts are common to anti-blooming devices. These features apply a bias to the charge sink means to make the device operate. Transcript at 44. He explained that the patent does not restrict the point of contact or the number of contacts to apply a bias to the charge sink means. According to Dr. Barbe, "a contact can be anything from a discrete point to-the complete bottom of a substrate.... So [a contact] can be looked at as a single point or as a continuum of points representing a large area." Transcript at 45. Dr. Barbe explained on cross-examination that the contact is generally made from an ohmic contact in the semiconductor and a metallic contact. Transcript at 99. As Dr. Barbe explained, a contact might be any point from or to which charge would flow. Transcript at 101.

The broad definition of "contact" in the specification, coupled with the testimony of Dr. Barbe, show that "a contact" is one or more paths for charge to flow to and from the charge sink means.

D. How does the charge sink means extend laterally?

[21] Finally, the parties interpret differently the phrase "extending laterally from said contact toward said light sensing element." The term "extending laterally" conveys a directional meaning. The specification and prosecution history provide little guidance for detecting the precise compass reading for this direction. However, that direction must run from the contact toward the light sensing element. Thus, the charge sink means, as interpreted by the court, must extend parallel to the top surface and perpendicular to a contact toward the light sensing element.

CONCLUSION

The court will enter an Order in accordance with this Opinion setting forth the meaning of the disputed portions of the claims.

ORDER CONSTRUING CLAIMS

For the reasons set forth in the Opinion of this date on claim construction, IT IS HEREBY ORDERED as follows:

A. As to United States Patent 3,931,674, the court finds:

1. In claim 1, "selectively applying at least one layer of insulation material to said semiconductor substrate" describes a process step during which one or more layers of insulation material of a defined thickness form at specific locations on the top surface of the silicon wafer.

2. Claim 1 describes a process that implants a barrier region in the semiconductor substrate using an insulated gate as a mask. In other words, the insulation material must be in place before implantation of the barrier region.

3. In claim 1, "said uppermost surface of said at least one insulating layer" requires formation of the second gate electrodes between the first gate electrodes on the upper surface of the same continuous insulation layer upon which the first gate electrodes were formed.

4. In claim 1, "connecting each of said second gate electrodes to an individual adjacent first gate electrode to form a composite electrode for a charge coupled element" describes a process step which connects each second gate electrode to one, but not both, adjacent first gate electrodes.

B. As to United States Patent 3,896,485, the court finds:

1. "[C]harge sink means" describes a means plus function limitation under 35 U.S.C. s. 112, para. 6. The specification describes the structure of the charge sink means as a region of semiconductor material doped opposite from its surrounding semiconductor material. The charge sink means does not include its associated depletion region.

2. "[B]uried within" requires the charge sink means to be completely surrounded by semiconductor material

and not in contact with any surface of the device.

3. "[A] contact" is one or more paths for charge to flow to and from the charge sink means.

4. "[E]xtending laterally from said contact toward said light sensing element" requires the charge sink means to extend parallel to the top surface and perpendicular to a contact toward the light sensing element.

E.D.N.Y.,1995.
Loral Fairchild Corp. v. Victor Co. of Japan, Ltd.

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